Intel® Desktop Board D810E2CA3

Technical Product Specification

February 2001

Order Number A43979-001

The Intel® Desktop Board D810E2CA3 may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board D810E2CB Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the Intel® Desktop Board D810E2CA3 Technical Product Specification	February 2001

This product specification applies only to the standard D810E2CA3 board with BIOS identifier CA81030A.86A.

Changes to this specification will be published in the D810E2CA3 Monthly Specification Update before being incorporated into a revision of this document.

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and BIOS for the Intel® D810E2CA3 desktop board. It describes the standard board product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the board and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on this board
2	A map of the resources of the board
3	The features supported by the BIOS Setup program
4	The contents of the BIOS Setup program's menus and submenus
5	A description of the BIOS error messages, beep codes, and Power-On Self-Test (POST) codes

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions that, if not observed, can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#).
(NxnX)	When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the board, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area.
GB	Gigabyte (1,073,741,824 bytes)
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
kbits/sec	1000 bits per second
MB	Megabyte (1,048,576 bytes)
MB/sec	Megabytes per second
Mbit	Megabit (1,048,576 bits)
Mbit/sec	Megabits per second
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
†	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

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4 BIOS Setup Program

5 Error Messages and Beep Codes

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Tables

1 Desktop Board Description

What This Chapter Contains

1.1 Overview

1.1.1 Feature Summary

Table 1 summarizes the D810E2CA3 board's major features.

Table 1. Feature Summary

Form Factor	microATX (9.6 inches by 8.0 inches)
Processor	Support for either an Intel® Pentium® III processor in a Flip Chip Pin Grid Array (FC-PGA) package or an Intel® Celeron™ processor in an FC-PGA package or a PPGA package
Memory	• Two 168-pin Dual Inline Memory Module (DIMM) sockets • Support for up to 512 MB of 100 MHz non-ECC, unbuffered synchronous DRAM (SDRAM) • Support for serial presence detect (SPD) and non-SPD DIMMs
Chipset	The Intel® 810E2 chipset, consisting of: • Intel® 82810E DC-133 Graphics and Memory Controller Hub (GMCH) • Intel® 82801BA I/O Controller Hub (ICH2) • SST 49LF004A 4 Mbit firmware hub (FWH)
I/O Control	SMSC LPC47M102 low pin count (LPC) interface I/O controller
Video	Intel 82810E DC-133 Graphics and Memory Controller Hub (integrated in the chipset) with an optional 4 MB of 133 MHz display cache
Audio	• Intel 82801BA ICH2 digital controller (AC link output) • Analog Devices AD1885 Audio Codec
Peripheral Interfaces	• Four Universal Serial Bus (USB) ports • Two IDE interfaces with Ultra DMA, ATA-66/100 support • One diskette drive interface • Two serial ports • One parallel port • PS/2 keyboard and mouse ports
Expansion Capabilities	Four PCI-bus add-in card connectors
BIOS	• Intel/AMI BIOS stored in an SST 49LF004A 4 Mbit firmware hub (FWH) • Support for SMBIOS, Advanced Configuration and Power Management Interface (ACPI), Advanced Power Management (APM), and Plug and Play
Instantly Available PC	• Support for *PCI Local Bus Specification Revision 2.2* • Suspend to RAM support • Wake on PS/2† keyboard and USB ports

For information about	Refer to
The board's compliance level with ACPI, APM, Plug and Play, and SMBIOS	Table 3, page 16

1.1.2 Manufacturing Options

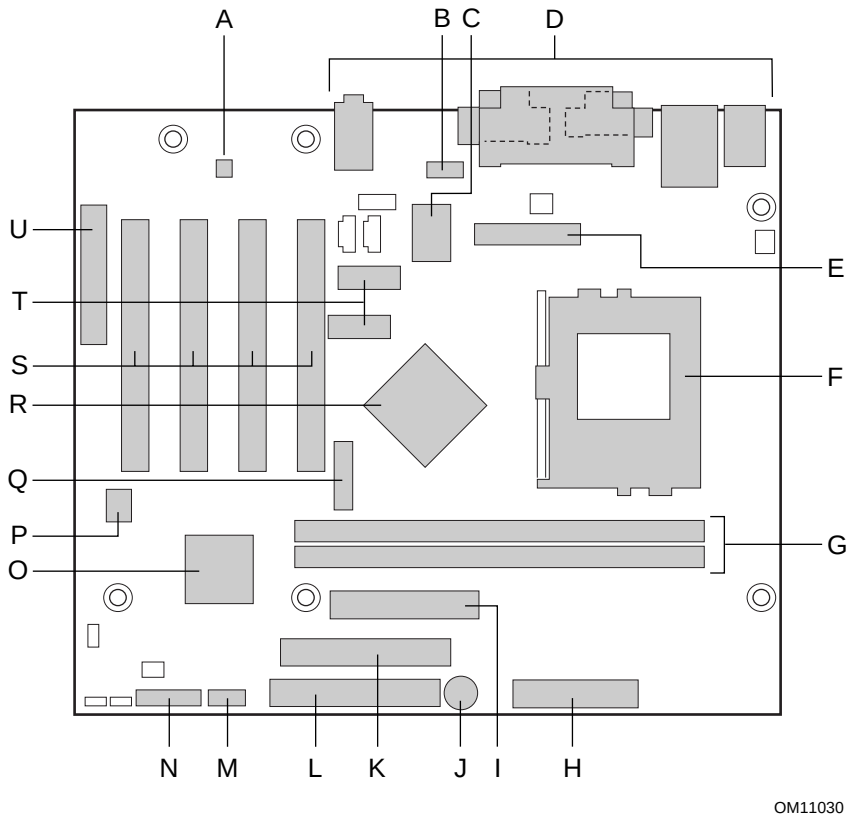
Table 2 describes the board's manufacturing options. Not all of the following manufacturing options are available in all marketing channels. Please contact your Intel representative to determine what manufacturing options are available to you.

Table 2. Manufacturing Options

Video	Digital video output (DVO) connector
Hardware Monitor Subsystem	• Wired for Management (WfM) compliant • Voltage sensor to detect out of range values
Communication and Networking Riser (CNR) Connector	One CNR connector (shared with slot 4)
LAN Subsystem	Intel® 82562ET 10/100 Mbit/sec Platform LAN Connect (PLC) device
Wake on LAN† Technology Connector	Support for system wake up using an add-in network interface card with remote wake up capability

1.1.3 Board Layout

Figure 1 shows the major components of the D810E2CA3 desktop board.



A	AD1885 audio codec	M	Front panel USB
B	Serial port B connector	N	Front panel connector
C	SMSC LPC47M102 I/O controller	O	Intel 82801BA I/O Controller Hub (ICH2)
D	Back panel connectors	P	Intel® 82802AB Firmware Hub (FWH)
E	DVO connector (optional)	Q	Battery
F	Processor socket	R	Intel 82810E DC-133 Graphics and Memory Controller Hub (GMCH)
G	DIMM sockets		
H	Power connector	S	PCI bus add-in card connectors
I	Diskette drive connector	T	4 MB display cache (optional)
J	Speaker	U	Communications and Networking Riser (CNR) connector (optional)
K	Secondary IDE connector		
L	Primary IDE connector		

Figure 1. D810E2CA3 Board Components

1.1.4 Block Diagram

Figure 2 is a block diagram of the major functional areas of the D810E2CA3 board.

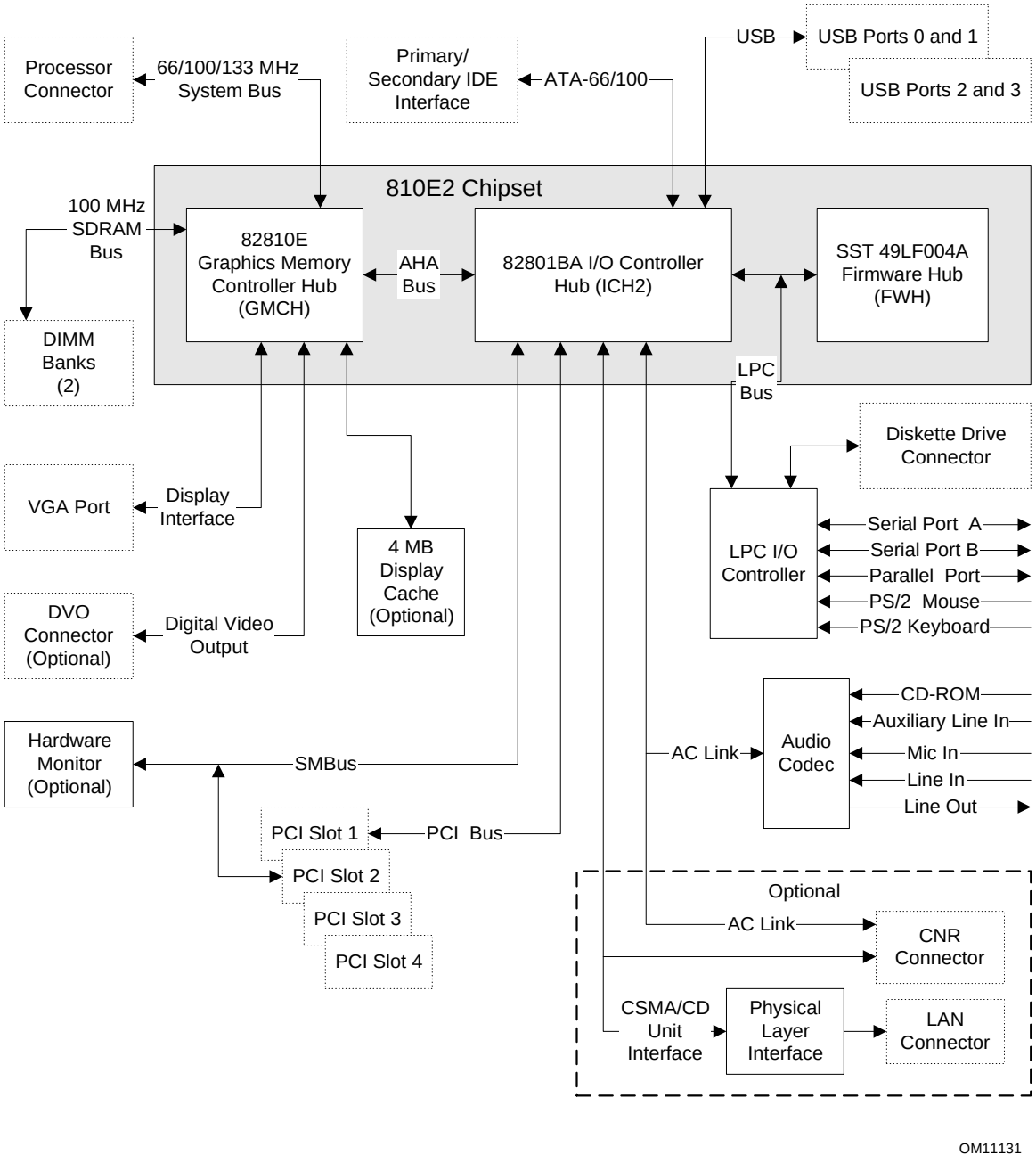


Figure 2. Board Block Diagram

1.2 Online Support

To find information about…	Visit this World Wide Web site:
Intel's D810E2CA3 board under "Product Info" or "Customer Support"	http://www.intel.com/design/motherbd/ http://support.intel.com/support/motherboards/desktop
Processor data sheets	http://www.intel.com/design/litcentr
Proper date access in systems with Intel® motherboards	http://support.intel.com/support/year2000
ICH2 addressing	http://developer.intel.com/design/chipsets/datashts
Custom splash screens	http://intel.com/design/motherbd/gen_indx.htm
Audio software and utilities	http://www.intel.com/design/motherbd
LAN software and drivers	http://www.intel.com/design/motherbd
Graphics software and utilities	http://www.intel.com/design/motherbd

1.3 Design Specifications

Table 3 lists the specifications applicable to the D810E2CA3 board.

Table 3. Specifications

Reference Name	Specification Title	Version, Revision Date, and Ownership	The information is available from…
AC '97	*Audio Codec '97*	Version 2.1, May 1998, Intel Corporation.	ftp://download.intel.com/ial/scalableplatforms/ac97r22.pdf
ACPI	*Advanced Configuration and Power Interface Specification*	Version 2.0, July 27, 2000, Compaq Computer Corp., Intel Corporation, Microsoft Corporation, and Toshiba Corporation.	http://www.teleport.com/~acpi/
AGP	*Accelerated Graphics Port Interface Specification*	Version 2.0, May 4, 1998, Intel Corporation.	http://www.agpforum.org/
AMI BIOS	*American Megatrends BIOS Specification*	AMIBIOS 99, 1999, American Megatrends, Inc.	http://www.amij.com/amibios/bios.platforms.desktop.html
APM	*Advanced Power Management BIOS Interface Specification*	Version 1.2, February 1996, Intel Corporation, Microsoft Corporation.	http://www.microsoft.com/hwdev/busbios/amp_12.htm
ATA/ ATAPI-5	*Information Technology - AT Attachment with Packet Interface -5, (ATA/ATAPI-5)*	Revision 3 February 29, 2000, Contact: T13 Chair, Seagate Technology	http://www.t13.org

continued

Table 3. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	The information is available from…
ATX	*ATX Specification*	Version 2.03, December 1998, Intel Corporation.	http://www.teleport.com/ ~ffsupprt/
BIS	Boot Integrity Services	Version 1.0 for WfM 2.0, August 1999, Intel Corporation.	http://developer.intel.com/ design/security/bis/ bisfaq.htm
CNR	*Communication and Network Riser (CNR) Specification*	Version 1.1, October 18, 2000, Intel Corporation.	http://developer.intel.com/ technology/cnr/index.htm
DVI	*Digital Visual Interface DVI*	Revision 1.0, April 2, 1999, Intel Corporation, Silicon Image Incorporated, Compaq Computer Corporation, Fujitsu Limited, Hewlett-Packard, and NEC Corporation.	http://www.ddwg.org/ downloads.html
EPP	*IEEE std 1284.1-1997* Enhanced Parallel Port	Version 1.7, 1997, Institute of Electrical and Electronic Engineers.	http://standards.ieee.org/ reading/ieee/std_public/ description/busarch/ 1284.1-1997_desc.html
El Torito	*Bootable CD-ROM Format Specification*	Version 1.0, January 25, 1995, Phoenix Technologies Ltd., and IBM Corporation.	http://www.ptltd.com/ techs//specs.html
LPC	*Low Pin Count Interface Specification*	Version 1.0, September 29, 1997, Intel Corporation.	http://www.intel.com/ design/chipsets/industry/ lpc.htm
PCI	*PCI Local Bus Specification*	Version 2.2, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/
	PCI Bus Power Management Interface Specification	Version 1.1, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/
Plug and Play	*Plug and Play BIOS Specification*	Version 1.0a, May 5, 1994, Compaq Computer Corp., Phoenix Technologies Ltd., and Intel Corporation.	http://www.microsoft.com/ hwdev/respec/ pnpspecs.htm
PXE	*Preboot Execution Environment*	Version 2.1, September 1999, Intel Corporation.	http://developer.intel.com/ ial/WfM/wfm20/design/ mapxe/index.htm

continued

Table 3. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	The information is available from…
SDRAM	PC SDRAM Unbuffered DIMM Specification	Revision 1.0, February 1998, Intel Corporation.	http://www.intel.com/design/chipsets/memory
	PC SDRAM DIMM Specification	Revision 1.7, November 1999, Intel Corporation.	http://www.intel.com/technology/memory
	PC Serial Presence Detect (SPD) Specification	Revision 1.2B, November 1999, Intel Corporation.	http://www.intel.com/technology/memory
SMBIOS	*System Management BIOS*	Version 2.3.1, March 16, 1999, American Megatrends Inc., Award Software International Inc., Compaq Computer Corporation Dell Computer Corporation, Hewlett-Packard Company, Intel Corporation, International Business Machines Corporation, Phoenix Technologies Limited, and SystemSoft Corporation.	http://developer.intel.com/ial/wfm/design/smbios
UHCI	*Universal Host Controller Interface Design Guide*	Version 1.1, March 1996, Intel Corporation.	http://www.usb.org/developers
USB	*Universal Serial Bus Specification*	Version 1.1, September 23, 1998, Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, and NEC Corporation.	http://www.usb.org/developers
WfM	*Wired for Management Baseline*	Version 2.0, December 18, 1998, Intel Corporation.	http://developer.intel.com/ial/WfM/wfmspecs.htm

1.4 Processor

CAUTION

Use only the processors listed below. Use of unsupported processors can damage the D810E2CA3 board, the processor, and the power supply. See the Intel Desktop Board D810E2CA3 Specification Update *for the most up-to-date list of supported processors for the D810E2CA3 board.*

The D810E2CA3 board supports either an Intel Pentium III processor (FC-PGA package), or an Intel Celeron processor (PGA package). The system bus speed is automatically selected. The board supports the processors listed in Table 4.

Table 4. Supported Processors

Processor Speed	Processor Speed	System Bus Frequency	L2 Cache Size
Pentium III processor	500E, 550E, 600, 650, 700, 750, 800, and 850 MHz	100 MHz	256 KB
	533EB, 600EB, 667, 733, 800EB, 866, and 933 MHz	133 MHz	256 KB
	1.0B GHz	133 MHz	256 KB
Celeron processor in an FC-PGA package	400, 433, 466, 500, 533A, 566A, 600, 633, 667, 700, 733, and 766 MHz	66 MHz	128 KB
	800 MHz	100 MHz	128 KB

All supported onboard memory can be cached, up to the cachability limit of the processor. See the processor's data sheet for cachability limits.

For information about	Refer to
Processor support	Section 1.2, page 16
Processor data sheets	Section 1.2, page 16

1.5 System Memory

⚠ CAUTION

Before installing or removing memory, disconnect AC power by unplugging the power cord from the computer. Failure to do so could damage the memory and the board.

NOTE

To be fully compliant with all applicable Intel® SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. If your memory module does not support SPD, you will see a notification to this effect on the screen at power-up. The BIOS will attempt to configure the memory controller for normal operation; however, DIMMs may not function at the determined frequency.

NOTE

Because the main system memory is also used as video memory, the board requires 66 MHz or 100 MHz SDRAM DIMMs. It is highly recommended that SPD DIMMs be used, since this allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted.

The board has two DIMM sockets. SDRAM can be installed in one or both sockets. Minimum memory size is 64 MB; maximum memory size is 512 MB. The BIOS automatically detects memory type, size, and speed. Due to the video requirements of the D810E2CA3 board, most configurations require at least 64 MB of memory.

The board supports memory with the following features:

- 3.3V, 168-pin DIMMs with gold-plated contacts
- 100 MHz unbuffered SDRAM
- Non-ECC (64-bit) memory
- Serial Presence Detect (SPD) or non-SPD memory (BIOS recovery requires SPD DIMMs)
- Unbuffered single- or double-sided DIMMs

This board is designed to support DIMM configurations listed in Table 4 below.

Table 5. System Memory Configurations

DIMM Size	Non-ECC Configuration
16 MB	2 Mbit x 64
32 MB	4 Mbit x 64
64 MB	8 Mbit x 64
128 MB	16 Mbit x 64
256 MB (Note)	32 Mbit x 64

Note: A 256 MB DIMM used with this board must be built with 128 Mbit device technology.

For information about	Refer to
The *PC Serial Presence Detect Specification*	Section 1.3, page 16
Obtaining copies of PC SDRAM specifications	http://www.intel.com/design/pcisets/memory

1.6 Intel® 810E2 Chipset

The Intel 810E2 chipset consists of the following devices:

- 82810E DC-133 Graphics Memory Controller Hub (GMCH) with accelerated hub architecture (AHA) bus
- 82801BA I/O Controller Hub (ICH2) with AHA bus
- SST 49LF004A 4 Mbit firmware hub (FWH)

The GMCH is a centralized controller for the system bus, the memory bus, the AGP bus, and the Accelerated Hub Architecture bus. The ICH2 is a centralized controller for the board's I/O paths. The FWH provides the nonvolatile storage of the BIOS. The component combination provides the interfaces as shown in Figure 3.

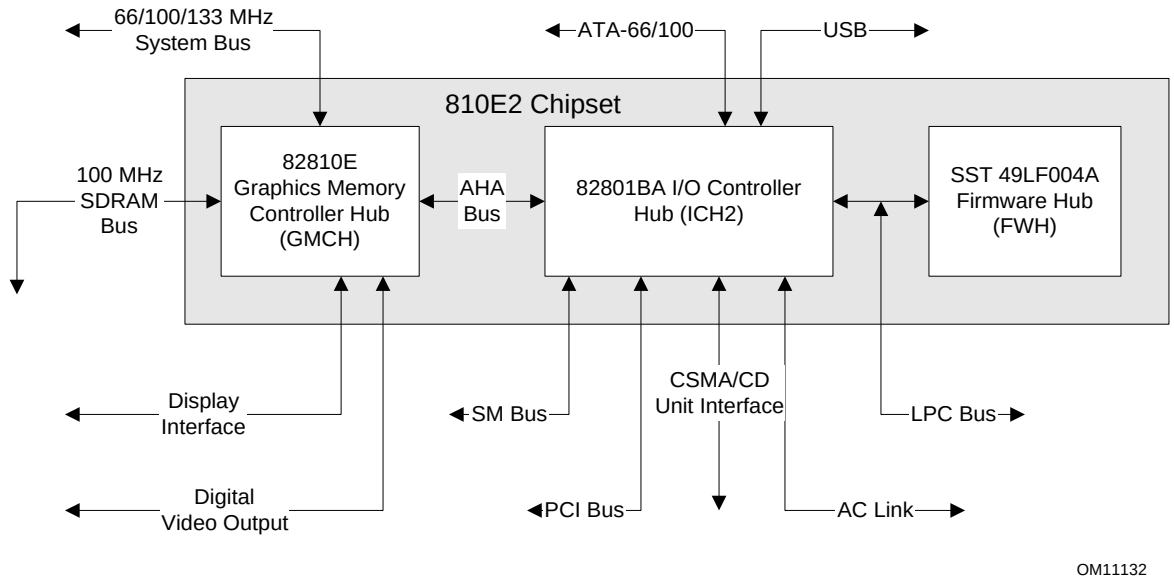


Figure 3. Intel 810E2 Chipset Block Diagram

For information about	Refer to
The Intel 810E2 chipset	http://developer.intel.com
The resources used by the chipset	Chapter 2
The chipset's compliance with ACPI, APM, AC '97	Section 1.3, page 16

1.6.1 USB

The ICH2 contains two separate USB controllers supporting four USB ports. Two of the ports are accessible through stacked back panel connectors and the other two are accessible through the front panel USB connector at location J8B1. One USB peripheral can be connected to each port. For more than four USB devices, an external hub can be connected to any of the ports. The board fully supports Universal Hub Controller Interface (UHCI) and uses UHCI-compatible software drivers.

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device or a low-speed USB device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

For information about	Refer to
The location of the back panel USB connectors	Figure 8, page 49
The signal names of the USB connectors	Table 21, page 50
The location of the front panel USB connector	Figure 11, page 63
The signal names of the front panel USB connector	Table 41, page 64
The USB and UHCI specifications	Section 1.3, page 16

1.6.2 IDE Interfaces

The ICH2's IDE controller has two independent bus-mastering IDE interfaces that can be independently enabled. The IDE interfaces support the following modes:

- Programmed I/O (PIO): processor controls data transfer.
- 8237-style DMA: DMA offloads the processor, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec.
- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible. ATA-66 uses faster timings and requires a specialized cable to reduce reflections, noise, and inductive coupling.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The ICH2 ATA-100 logic can achieve read transfer rates up to 100 MB/sec and write transfer rates up to 88 MB/sec.

NOTE

ATA-100 and ATA-66 use faster timings and require a specialized cable to reduce reflections, noise, and inductive coupling.

The IDE interfaces also support ATAPI devices (such as CD-ROM drives) and ATA devices using the transfer modes listed in Table 66 on page 95.

The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The D810E2CA3 board supports Laser Servo (LS-120) diskette technology through its IDE interfaces. An LS-120 drive can be configured as a boot device by setting the BIOS Setup program's Boot menu to one of the following:

- ARMD-FDD (ATAPI removable media device – floppy disk drive)
- ARMD-HDD (ATAPI removable media device – hard disk drive)

For information about	Refer to
The location of the IDE connectors	Figure 10, page 58
The signal names of the IDE connectors	Table 39, page 62
BIOS Setup program's Boot menu	Table 72, page 101

1.6.3 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock is compatible with DS1287 and MC146818 components. The clock provides a time-of-day clock and a multicentury calendar with alarm features and century rollover. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

The time, date, and CMOS values can be specified in the Setup program. The CMOS values can be returned to their defaults by using the Setup program.

NOTE

If the battery and AC power fail, custom defaults, if previously saved, will be loaded into CMOS SRAM at power on.

A coin-cell battery powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the 3.3 V standby current extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 V applied.

For information about	Refer to
The location of the battery	Figure 1, page 14
Proper date access in systems with Intel desktop boards	Section 1.2, page 16

1.6.4 SST 49LF004A 4 Mbit Firmware Hub (FWH)

The FWH provides the following:

- System BIOS
- System security and manageability logic that enables protection for storing and updating of platform information

1.7 I/O Controller

The SMSC LPC47M102 I/O controller provides the following features:

- Low pin count (LPC) interface
- 3.3 V operation
- Two serial ports
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- PS/2–style mouse and keyboard interfaces
- Interface for one 1.2 MB, 1.44 MB, or 2.88 MB diskette drive
- Intelligent power management, including a programmable wake up event interface
- PCI power management support
- GPIO controlled on/off processor fan

The BIOS Setup program provides configuration options for the I/O controller.

For information about	Refer to
SMSC LPC47M102 I/O controller	http://www.smsc.com

1.7.1 Serial Ports

The D810E2CA3 board has two serial ports. Serial port A is located on the back panel. Serial port B is accessible using the connector at location J1E2. The serial ports' NS16C550-compatible UARTs support data transfers at speeds up to 115.2 kbits/sec with BIOS support. The serial ports can be assigned as COM1 (3F8h), COM2 (2F8h), COM3 (3E8h), or COM4 (2E8h).

For information about	Refer to
The location of the serial port A connector	Figure 8, page 49
The signal names of the serial port A connector	Table 24, page 52
The location of the serial port B connector	Figure 11, page 63
The signal names of the serial port B connector	Table 40, page 64

1.7.2 Parallel Port

The connector for the multimode bidirectional parallel port is a 25-pin D-Sub connector located on the back panel of the board. In the Setup program, there are four options for parallel port operation:

- Output Only (PC AT†-compatible mode)
- Bi-directional (PS/2 compatible)
- EPP
- ECP

For information about	Refer to
The location of the parallel port connector	Figure 8, page 49
The signal names of the parallel port connector	Table 23, page 51

1.7.3 Diskette Drive Controller

The I/O controller supports a single diskette drive that is compatible with the 82077 diskette drive controller and supports both PC-AT† and PS/2 modes.

NOTE

The I/O controller supports 1.2 MB, 3.5-inch diskette drives, but a special driver is required for this type of drive.

For information about	Refer to
The location of the diskette drive connector	Figure 10, page 58
The signal names of the diskette drive connector	Table 38, page 61
The supported diskette drive capacities and sizes	Table 67, page 96

1.7.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel of the board. The +5 V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, reestablishes the connection after an overcurrent condition is removed.

NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains code that provides the traditional keyboard and mouse control functions and also supports power-on/reset password protection. A power-on/reset password can be specified in the BIOS Setup program.

The keyboard controller also supports the hot-key sequence <Ctrl><Alt><Del> for a software reset (operating system dependent). This key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the power-on self-test (POST).

For information about	Refer to
The location of the keyboard and mouse connectors	Figure 8, page 49
The signal names of the keyboard and mouse connectors	Table 19, page 50

1.8 Graphics Subsystem

1.8.1 Integrated Graphics Controller

The Intel 82810E DC-133 Graphics and Memory Controller Hub (GMCH) component provides the following graphics support features:

- Integrated graphics controller
  - 3-D Hyper Pipelined architecture
  - Full 2-D hardware acceleration
  - Motion video acceleration
- 3-D graphics visual and texturing enhancements
- Display
  - Integrated 24-bit 230 MHz RAMDAC
  - Display Data Channel Standard, Version 3.0, Level 2B protocols compliant (see Section 1.3 for specification information)
- Video
  - Hardware motion compensation for software MPEG2 decode
  - Software DVD at 30 fps
- Integrated graphics memory controller
- 4 MB of 133 MHz onboard video display cache (optional)

For information about	Refer to
The GMCH	Section 1.2, page 16
Obtaining graphics software and utilities	Section 1.2, page 16

Table 6 lists the refresh rates supported by the D810E2CA3 board.

Table 6. Supported Graphics Refresh Frequencies

Resolution	Color Palette	Available Refresh Frequencies (Hz)	Notes
320 x 200	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
320 x 240	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
352 x 480	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
352 x 576	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
400 x 300	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
512 x 384	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
640 x 400	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
640 x 480	256 colors	60, 70, 72, 75, 85	KDO
	64 K colors	60, 75, 85	KD3O
	64 K colors	70, 72	KDO
640 x 480	16 M colors	60, 70, 72, 75, 85	KDO
800 x 600	256 colors	60, 70, 72, 75, 85	KDO
	64 K colors	60, 70, 72, 75, 85	KD3O
	16 M colors	60, 70, 72, 75, 85	KDO
1024 x 768	256 colors	60, 70, 75, 85	KDO
	64 K colors	60, 70, 75	KD3O
	64 K colors	85	KD3
	16 M colors	60, 70, 75, 85	KD

continued

Table 6. Supported Graphics Refresh Frequencies (continued)

Resolution	Color Palette	Available Refresh Frequencies (Hz)	Notes
1152 x 864	256 colors	60, 70, 72, 75	KDO
	256 colors	85	KD
	64 K colors	60, 70	KD3O
	64 K colors	72, 75, 85	KD3
	16 M colors	60	KDO
	16 M colors	75, 85	KD
1280 x 768	256 colors	60 (reduced blanking)	KDOF
	64 K colors	60 (reduced blanking)	KD3F
	16 M colors	60 (reduced blanking)	KDF
1280 x 1024	256 colors	60	KDO
	256 colors	70, 72, 75, 85	KD
	64 K colors	60, 70, 72, 75, 85	KD3
	16 M colors	60, 70, 75, 85	KD
1600 x 1200	256 colors	60, 70, 72, 75	KD

Notes: K = Desktop
D = DirectDraw†
3 = Direct3D† and OpenGL†
O = Overlay
F = Digital Display Device only. A mode will be supported on both analog CRTs and digital display devices (KD3O applies to both types of displays), unless indicated otherwise.

NOTE

Some of the system memory is reserved for video.

1.8.2 Digital Video Output (DVO) Connector (Optional)

The board routes the Intel 82810E GMCH DVO port to an onboard 40-pin DVO connector. The DVO connector can be cabled to a DVI or TV out card to enable digital displays or TV out functionality. The Digital Visual Interface (DVI) specification provides a high-speed digital connection for visual data types when using the integrated graphics controller. This interface is active only when the integrated graphics controller is enabled.

The DVI interface allows interfacing with a discrete Transmission Minimized Differential Signaling (TMDS) transmitter to enable platform support for DVI compliant digital displays or with a discrete TV encoder for TV out functionality.

For information about	Refer to
The location of the DVO connector	Figure 9, page 54
The signal names of the DVO connector	Table 31, page 56
Obtaining the DVI specification	Table 3, page 16

1.9 Audio Subsystem

The board includes an Audio Codec ’97 (AC ’97) compatible audio subsystem consisting of these devices:

- Intel 82801BA ICH2 digital controller (AC link output)
- Analog Devices AD1885 analog codec

Features of the audio subsystem include:

- Split digital/analog architecture for improved S/N (signal-to-noise) ratio: ≥ 85 dB
- 3-D stereo enhancement
- Power management support for APM 1.2 and ACPI 2.0 (driver dependent)

The audio subsystem supports the following audio connectors:

- Inputs:
  - Three analog line-level stereo inputs for connection from line in, CD, and auxiliary line in
  - One mono microphone input
- Output: Stereo line-level output

For information about	Refer to
Obtaining audio software and utilities	Section 1.2, page 16
Obtaining the AC ’97 specification	Table 3, page 16

1.9.1 AD1885 Analog Codec

The AD1885 is a fully AC ’97 compliant codec. The codec’s features include:

- > 90 dB signal-to-noise ratio sound quality
- Power management support for APM 1.2 and ACPI 2.0 (driver dependent)
- Playback sample rates up to 48 kHz
- 16 bit stereo full-duplex operation
- Software compatible with Windows† 98 SE, Windows 2000, Windows Millennium Edition (Windows Me), and Windows NT† 4.0
- Full-duplex operation at asynchronous hardware record/playback sample rates
- Frequency response: 20 Hz to 20 kHz (± 0.1 dB)

Figure 4 is a block diagram of the board’s audio subsystem, including the Intel 82801BA ICH2 digital controller, the AD1885 analog codec, and the audio connectors.

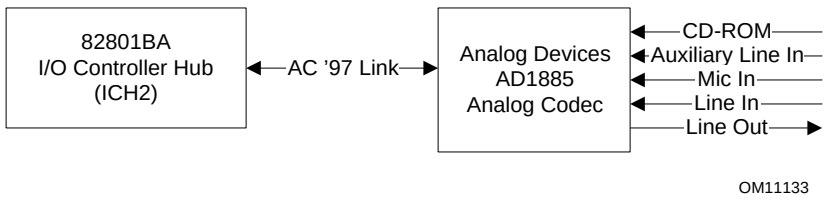


Figure 4. Block Diagram of Audio Subsystem

1.9.2 Audio Connectors

The audio connectors include the following:

- ATAPI-style connectors:
  - CD-ROM
  - Auxiliary line in
- Front panel audio
- Back panel connectors:
  - Line out
  - Line in
  - Mic in

NOTE

The line out connector, located on the back panel, is designed to power either headphones or amplified speakers only. Poor audio quality may occur if passive (non-amplified) speakers are connected to this output.

For information about	Refer to
The back panel audio connectors	Section 2.8.1, page 49

1.9.2.1 ATAPI CD-ROM Audio Connector

A 1 x 4-pin ATAPI-style connector connects an internal ATAPI CD-ROM drive to the audio mixer.

For information about	Refer to
The location of the ATAPI CD-ROM connector	Figure 9, page 54
The signal names of the ATAPI CD-ROM connector	Table 28, page 55

1.9.2.2 Front Panel Audio Connector

A 2 x 5-pin connector for routing mic in and line out to the front panel.

For information about	Refer to
The location of the front panel audio connector	Figure 9, page 54
The signal names of the front panel audio connector	Table 29, page 55

1.9.2.3 Auxiliary Line In Connector

A 1 x 4-pin ATAPI-style connector connects the left and right channel signals of an internal audio device to the audio subsystem.

For information about	Refer to
The location of the auxiliary line in connector	Figure 9, page 54
The signal names of the auxiliary line in connector	Table 30, page 55

1.10 LAN Subsystem (Optional)

The Network Interface Controller subsystem consists of the ICH2, with integrated LAN Media Access Controller (MAC), and a physical layer interface device. Features of the LAN subsystem include:

- PCI Bus Master Interface
- CSMA/CD Protocol Engine
- Serial CSMA/CD unit interface that supports the 82562ET (10/100 Mbit/sec Ethernet) physical layer interface device
- PCI Power Management
  - — Supports APM
  - — Supports ACPI technology
  - — Supports Wake up from suspend state (Wake on LAN technology)

For information about	Refer to
Obtaining LAN software and drivers	Section 1.2, page 16

1.10.1 Intel® 82562ET Platform LAN Connect Device

The Intel 82562ET component provides an interface to the back panel RJ-45 connector with integrated LEDs. This physical interface may alternately be provided using the CNR connector.

The Intel 82562ET provides the following functions:

- Basic 10/100 Ethernet LAN Connectivity
- Supports RJ-45 connector with status indicator LEDs
- Full driver compatibility
- Advanced Power Management support
- Programmable transit threshold
- Configuration EEPROM that contains the MAC address

1.10.2 RJ-45 LAN Connector LEDs

Two LEDs are built into the RJ-45 LAN connector. Table 7 describes the LED states when the board is powered up and the LAN subsystem is operating.

Table 7. LAN Connector LED States

LED Color	LED State	Condition
Green	Off	10 Mbit/sec data rate is selected.
	On	100 Mbit/sec date rate is selected.
Yellow	Off	LAN link is not established.
	On (steady state)	LAN link is established.
	On (brighter and pulsing)	The computer is communicating with another computer on the LAN.

1.11 CNR (Optional)

The CNR connector supports the audio, modem, USB, and LAN interfaces of the Intel 810E2 chipset. Figure 5 shows the signal interface between the riser and the ICH2.

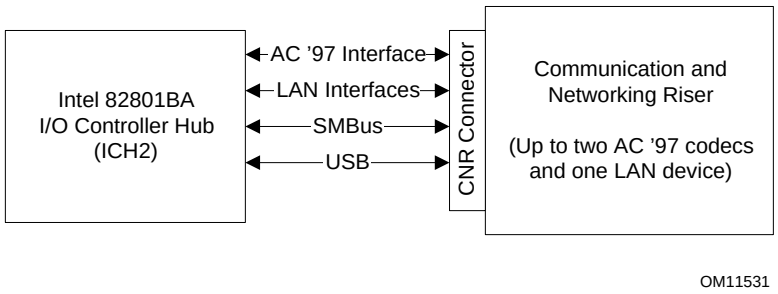


Figure 5. ICH2 and CNR Signal Interface

The interfaces supported by the CNR connector include (but are not limited to) the following:

- **AC '97 interface:** supports audio and/or modem functions on the CNR board.
- **LAN interfaces:** an eight-pin interface for use with Platform LAN Connection (PLC) based devices.
- **SMBus interface:** provides Plug-and-Play functionality for the CNR board.
- **USB interface:** provides a USB interface for the CNR board.

To learn more about the CNR, refer to the CNR specification.

For information about	Refer to
Obtaining the CNR specification	Section 1.3, page 16

CAUTION

Do not install a LAN CNR card if the D810E2CA3 board already has an onboard LAN subsystem. Doing so could prevent the board from connecting to the LAN.

1.12 Hardware Management Subsystem (Optional)

The hardware management features enable the board to be compatible with the Wired for Management (WfM) specification. The board has several hardware management features, including the following:

- Hardware monitor component
- Fan control and monitoring (implemented on the SMSC LPC47M102 I/O controller)

For information about	Refer to
The WfM specification	Section 1.3, page 16
Fan control functions of the SMSC LPC47M102 I/O controller	Section 1.12.2, page 33

1.12.1 Hardware Monitor Component

The optional hardware monitor component provides low-cost instrumentation capabilities. The features of the component include:

- Internal ambient temperature sensing
- Remote thermal diode sensing for direct monitoring of processor temperature
- Power supply monitoring (+12 V, +5 V, +3.3 V, +2.5 V, +3.3 VSB, and V_{CCP}) to detect levels above or below acceptable values
- SMBus interface

1.12.2 Fan Control and Monitoring

The SMSC LPC47M102 I/O controller provides one fan control output. The other fan is always active. Monitoring and control can be implemented using third-party software.

For information about	Refer to
The functions of the fan connectors	Section 1.13.2.2, page 39
The location of the fan connectors	Figure 9, page 54
The signal names of the fan connectors	Section 2.8.2.1, page 54

1.13 Power Management Features

Power management is implemented at several levels, including:

- Software support:
  - — Advanced Power Management (APM)
  - — Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - — Wake on LAN technology (optional)
  - — Instantly Available technology
  - — Resume on Ring
  - — Wake from USB
  - — Wake on Keyboard
  - — Wake on PME#

1.13.1 Software Support

The software support for power management includes:

- APM
- ACPI

If the board is used with an ACPI-aware operating system, the BIOS can provide ACPI support. Otherwise, it defaults to APM support.

1.13.1.1 APM

APM makes it possible for the computer to enter an energy saving standby mode. The standby mode can be initiated in the following ways:

- Time-out period specified in the BIOS Setup program
- From the operating system, such as the Suspend menu item in Windows 98

In standby mode, the board can reduce power consumption by spinning down hard drives, and reducing power to or turning off VESA† DPMS-compliant monitors. Power management mode can be enabled or disabled in the BIOS Setup program.

While in standby mode, the system retains the ability to respond to external interrupts and service requests, such as incoming faxes or network messages. Any keyboard or mouse activity brings the system out of standby mode and immediately restores power to the monitor.

The BIOS enables APM by default; but the operating system must support an APM driver for the power management features to work. For example, Windows 98 supports the power management features upon detecting that APM is enabled in the BIOS.

Table 8 lists the devices or specific events that can wake the computer from specific states.

Table 8. APM Wake Up Devices and Events

These devices/events can wake up the computer…	…from this state
Power switch	Soft-off
RTC alarm*	Soft-off, suspend
LAN	Soft-off, suspend
PME#	Soft-off, suspend
USB	Suspend
PS/2	Suspend

* Unattended Wake Mode – display will be video BIOS string only

For information about	Refer to
Enabling or disabling power management in the BIOS Setup program	Section 4.6, page 100
The board's compliance level with APM	Table 3, page 16

1.13.1.2 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with this board requires the support of an operating system that provides full ACPI functionality. ACPI features include:

- Plug and Play (including bus and device enumeration) and APM support normally contained in the BIOS.
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives.
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state, and less than 5-watt system operation in the Suspend to Disk sleeping state.
- A Soft-off feature that enables the operating system to power-off the computer.
- Support for multiple wake up events (see Table 11 on page 37).
- Support for a front panel power and sleep mode switch. Table 9 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 9. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off (ACPI G2/G5 – Soft off)	Less than four seconds	Power-on (ACPI G0 – working state)
On (ACPI G0 – working state)	Less than four seconds	Soft-off/Standby (ACPI G1 – sleeping state)
On (ACPI G0 – working state)	More than four seconds	Fail safe power-off (ACPI G2/G5 – Soft off)
Sleep (ACPI G1 – sleeping state)	Less than four seconds	Wake up (ACPI G0 – working state)
Sleep (ACPI G1 – sleeping state)	More than four seconds	Power-off (ACPI G2/G5 – Soft off)

NOTE

The optional Wake on LAN technology connector at location J7A1 is provided to support wake up from a LAN adapter in APM mode. Wake on LAN technology in ACPI mode is supported by the PME# signal on the PCI connector.

For information about	Refer to
The board's compliance level with ACPI	Section 1.3, page 16

1.13.1.2.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 10 lists the power states supported by the board along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 10. Power States and Targeted System Power

Global States	Sleeping States	CPU States	Device States	Targeted System Power (Note 1)
G0 - working state	S0 – working	C0 - working	D0 - working state	Full power > 30 W
G1 - sleeping state	S1 - CPU stopped	C1 - stop grant	D1, D2, D3 - device specification specific.	5 W < power < 30 W
G1 - sleeping state	S3 - Suspend-to-RAM Context saved to RAM	No power	D3 - no power except for wake up logic.	Power < 5 W (Note 2)
G2/S5	S5 - Soft off. Context not saved. Cold boot is required.	No power	D3 - no power except for wake up logic.	Power < 5 W (Note 2)
G3 - mechanical off AC power is disconnected from the computer.	No power to the system.	No power	D3 - no power for wake up logic, except when provided by battery or external source.	No power to the system so that service can be performed.

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

1.13.1.2.2 Wake Up Devices and Events

Table 11 lists the devices or specific events that can wake the computer from specific states.

Table 11. Wake Up Devices and Events

These devices/events can wake up the computer…	…from this state
Power switch	S1, S3, S5
RTC alarm	S1, S3, S5
LAN (S5 state requires a Wake on LAN technology connector)	S1, S3, S5
Modem	S1, S3
USB	S1, S3
PS/2 keyboard	S1, S3
PS/2 mouse	S1, S3
PME#	S1, S3

1.13.1.2.3 Plug and Play

In addition to power management, ACPI provides controls and information so that the operating system can facilitate Plug and Play device enumeration and configuration. ACPI is used only to enumerate and configure board devices that do not have other hardware standards for enumeration and configuration. PCI devices on the board, for example, are not enumerated by ACPI.

1.13.2 Hardware Support

⚠ CAUTION

If Wake on LAN and Instantly Available technology features are used, ensure that the power supply provides adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options. Refer to Section 2.11.3 on page 71 for additional information.

The board provides several hardware features that support power management, including:

- Power connector
- Fan connectors
- Wake on LAN technology (optional)
- Instantly Available technology
- Resume on Ring
- Wake from USB
- Wake from PS/2 keyboard
- PME# wakeup support

Wake on LAN technology and Instantly Available technology require power from the +5 V standby line. The sections discussing these features describe the incremental standby power requirements for each.

Resume on Ring enables telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal) and the power management mode being used (APM or ACPI).

NOTE

The use of Resume on Ring technology from an ACPI state requires the support of an operating system that provides full ACPI functionality.

1.13.2.1 Power Connector

When used with an ATX-compliant power supply that supports remote power on/off, the board can turn off the system power through software control. To enable soft-off control in software, advanced power management must be enabled in the BIOS Setup program and in the operating system. When the system BIOS receives the correct APM command from the operating system, the BIOS turns off power to the computer.

With soft-off enabled, if power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off). The computer's response can be set using the After Power Failure feature in the BIOS Setup program's Boot menu.

For information about	Refer to
The location of the power connector	Figure 9, page 54
The signal names of the power connector	Table 34, page 57
The BIOS Setup program's Boot menu	Table 72, page 101
The ATX specification	Section 1.3, page 16

1.13.2.2 Fan Connectors

The board has two fan connectors. The functions of these connectors are described in Table 12.

Table 12. Fan Connector Descriptions

Connector	Function
Processor fan (fan 1)	Provides +12 V DC for a processor fan or active fan heatsink.
Chassis fan (fan 2)	Provides +12 V DC for a system or chassis fan. The fan voltage can be switched on or off, depending on the power management state of the computer.

NOTE

The on/off control for fan 2 is only available with the hardware monitor option.

1.13.2.3 Wake on LAN Technology (Optional)

CAUTION

For Wake on LAN technology, the 5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Wake on LAN technology can damage the power supply. Refer to Section 2.11.3 on page 71 for additional information.

Wake on LAN technology enables remote wakeup of the computer through a network. The LAN subsystem, whether onboard or as a PCI bus network adapter, monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet† frame, the LAN subsystem asserts a wakeup signal that powers up the computer. Depending on the LAN implementation, the board supports Wake on LAN technology in the following ways:

- Through the Wake on LAN technology connector
- Through the PCI bus PME# signal (for PCI 2.2 compliant LAN designs)
- Through the onboard LAN subsystem when enabled in Setup (ACPI only)

The Wake on LAN technology connector can be used with PCI bus network adapters that have a remote wake up connector, as shown in Figure 6. Network adapters that are PCI 2.2 compliant assert the wakeup signal through the PCI bus signal PME# (pin A19 on the PCI bus connectors). The optional onboard LAN subsystem also supports remote wakeup using the PME# signal.

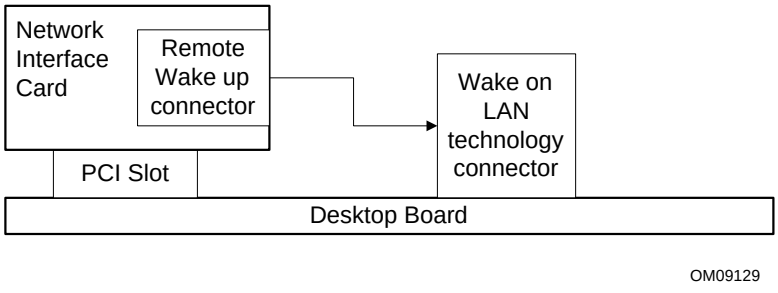


Figure 6. Using the Wake on LAN Technology Connector

For information about	Refer to
The location of Wake on LAN technology connector	Figure 9, page 54
The signal names of the Wake on LAN technology connector	Table 35, page 57

1.13.2.4 Instantly Available Technology

CAUTION

For Instantly Available technology, the 5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Instantly Available technology can damage the power supply. Refer to Section 2.11.3 on page 71 for additional information.

Instantly Available technology enables the board to enter the ACPI S3 (Suspend-to-RAM) sleep state. While in the S3 sleep state, the computer will appear to be off (the power supply is off, the fans are off, and the front panel LED is amber if dual-color, or off if single-color.) When signaled by a wake up device or event, the system quickly returns to its last known wake state. Table 11 on page 37 lists the devices and events that can wake the computer from the S3 state.

The board supports the *PCI Bus Power Management Interface Specification*. For information on the versions of this specification, see Section 1.3. Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

The use of Instantly Available technology requires operating system support and PCI 2.2 compliant add-in cards and drivers.

The standby power indicator (located between the DIMM sockets and the power connector) provides an indication that power is still present to the DIMMs and PCI bus connectors, even when the computer appears to be off.

Figure 7 shows the location of the standby power LED.

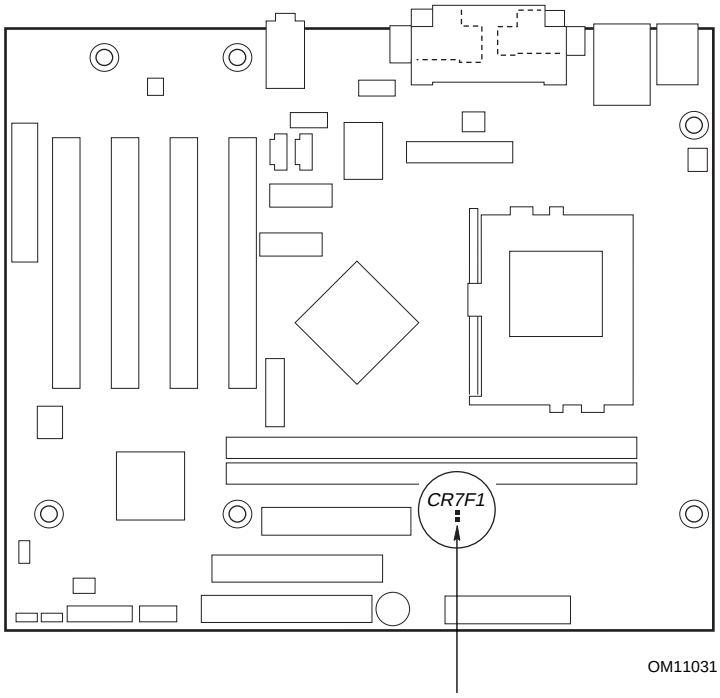


Figure 7. Location of Standby Power Indicator LED

1.13.2.5 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from either the APM sleep mode or the ACPI S1 state
- Requires only one call to access the computer
- Detects incoming call similarly for external and internal modems
- Requires modem interrupt be unmasked for correct operation

1.13.2.6 Wake from USB

USB bus activity wakes the computer from an ACPI S1 or S3 state.

NOTE

Wake from USB requires the use of a USB peripheral that supports Wake from USB.

1.13.2.7 Wake from PS/2 Keyboard

PS/2 keyboard activity wakes the computer from an ACPI S1 or S3 state.

1.13.2.8 PME# Wakeup Support

When the PME# signal on the PCI bus is asserted, the computer wakes from an ACPI S1 or S3 state.

2 Technical Reference

What This Chapter Contains

2.1 Introduction

Sections 2.2 – 2.6 contain several standalone tables. Table 13 describes the system memory map, Table 14 shows the I/O map, Table 15 lists the DMA channels, Table 16 defines the PCI configuration space map, and Table 17 describes the interrupts. The remaining sections in this chapter are introduced by text found with their respective section headings.

2.2 Memory Map

Table 13. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 524288 K	100000 - 1FFFFFFF	511 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Available high DOS memory (open to PCI bus)
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

2.3 I/O Map

Table 14. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	DMA controller
0020 - 0021	2 bytes	Programmable Interrupt Control (PIC)
0040 - 0043	4 bytes	System timer
0060	1 byte	Keyboard controller byte—reset IRQ
0061	1 byte	System speaker
0064	1 byte	Keyboard controller, CMD/STAT byte
0070 - 0071	2 bytes	System CMOS/Real Time Clock
0072 - 0073	2 bytes	System CMOS
0080 - 008F	16 bytes	DMA controller
0092	1 byte	Fast A20 and PIC
00A0 - 00A1	2 bytes	PIC
00B2 - 00B3	2 bytes	APM control
00C0 - 00DF	32 bytes	DMA
00F0	1 byte	Numeric data processor
0170 - 0177	8 bytes	Secondary IDE channel
01F0 - 01F7	8 bytes	Primary IDE channel
One of these ranges: 0220 - 022F 0240 - 024F	16 bytes	Audio (Sound Blaster Pro† -compatible)
0228 - 022F (Note 1)	8 bytes	LPT3
0278 - 027F (Note 1)	8 bytes	LPT2
02E8 - 02EF (Note 1)	8 bytes	COM4/video (8514A)
02F8 - 02FF (Note 1)	8 bytes	COM2
0376	1 byte	Secondary IDE channel command port
0377, bits 6:0	7 bits	Secondary IDE channel status port
0 378 - 037F	8 bytes	LPT1
0388 - 038B	6 bytes	AdLib† (FM synthesizer)
03B0 - 03BB	12 bytes	Intel 82810E DC-133 GMCH
03C0 - 03DF	32 bytes	Intel 82810E DC-133 GMCH
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5	6 bytes	Diskette channel 1
03F6	1 byte	Primary IDE channel command port
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
LPTn + 400	8 bytes	ECP port, LPTn base address + 400h
0CF8 - 0CFB (Note 2)	4 bytes	PCI configuration address register
0CF9 (Note 3)	1 byte	Turbo and reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register
FFA0 - FFA7	8 bytes	Primary bus master IDE registers
FFA8 - FFAF	8 bytes	Secondary bus master IDE registers
96 contiguous bytes starting on a 128-byte divisible boundary		ICH (ACPI + TCO)

continued

Table 14. I/O Map (continued)

Address (hex)	Size	Description
64 contiguous bytes starting on a 64-byte divisible boundary		D810E2CA3 Board resource
256 contiguous bytes starting on a 256-byte divisible boundary		AC ’97 audio mixer
64 contiguous bytes starting on a 64-byte divisible boundary		ICH2 LAN controller
256 contiguous bytes starting on a 256-byte divisible boundary		AC ‘97 modem mixer
64 contiguous bytes starting on a 64-byte divisible boundary		AC ‘97 audio mixer
32 contiguous bytes starting on a 32-byte divisible boundary		ICH2 (USB controller #1)
32 contiguous bytes starting on a 32-byte divisible boundary		ICH2 (USB controller #2)
16 contiguous bytes starting on a 16-byte divisible boundary		ICH2 (SMB)
4096 contiguous bytes starting on a 4096-byte divisible boundary		Intel 82801BA PCI bridge
64 contiguous bytes starting on a 64-byte divisible boundary		Intel 82562ET LAN controller (optional)

Notes:

1. Default, but can be changed to another address range.
2. Dword access only
3. Byte access only

NOTE

Some additional I/O addresses are not available due to ICH2 address aliassing.

For information about	Refer to
ICH2 addressing	Section 1.2, page 16

2.4 DMA Channels

Table 15. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8 or 16 bits	Open
1	8 or 16 bits	Parallel port
2	8 or 16 bits	Diskette drive
3	8 or 16 bits	Parallel port (for ECP or EPP)
4		DMA controller
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

2.5 PCI Configuration Space Map

Table 16. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Intel 82810E GMCH (memory controller hub)
00	01	00	Intel 82810E GMCH (graphics controller hub)
00	1E	00	Hub link to PCI bridge
00	1F	00	Intel 82801BA ICH2 (I/O controller hub) PCI to LPC bridge
00	1F	01	IDE
00	1F	02	USB controller #1
00	1F	03	SMBUS
00	1F	04	USB controller #2
00	1F	05	AC '97 audio controller or reserved
00	1F	06	AC '97 modem controller or reserved
01	08	00	Intel 82562ET LAN controller (optional)
01	09	00	PCI bus connector 1 (J3D1)
01	0A	00	PCI bus connector 2 (J3C1)
01	0B	00	PCI bus connector 3 (J3B1)
01	0C	00	PCI bus connector 4 (J3A2)

2.6 Interrupts

Table 17. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 (Note) (user available if COM2 is not present)
4	COM1 (Note)
5	LAN / user available
6	Diskette drive controller
7	LPT1 (Note)
8	Real time clock
9	User available
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

Note: Default, but can be changed to another IRQ

2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI expansion slots and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The ICH2 has eight programmable interrupt request (PIRQ) input signals. All PCI interrupt sources either onboard or from a PCI add-in card connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the D810E2CA3 board and therefore share the same interrupt. Table 18 shows an example of how the PIRQ signals are routed on the D810E2CA3 board. For example, using Table 18 as a reference, assume an add-in card using INTA is plugged into PCI bus connector 4. In PCI bus connector 4, INTA is connected to PIRQB, which is already connected to the SMBus. The add-in card in PCI bus connector 4 now shares interrupts with these onboard interrupt sources.

Table 18. PCI Interrupt Routing Map

PCI Interrupt Source	ICH PIRQ Signal Name				
	PIRQF	**PIRQG**	**PIRQC**	**PIRQB**	**Other**
GMCH				INTB	INTA to PIRQA
ICH2 USB controller #1					INTD to PIRQD
SMBus controller				INTB	
ICH2 USB controller #2					INTC to PIRQH
ICH2 Audio				INTB	
ICH2 LAN					INTA to PIRQE
PCI Bus Connector 1 (J3D1)	INTB	INTC	INTA	INTD	
PCI Bus Connector 2 (J3C1)	INTA	INTB	INTD	INTC	
PCI Bus Connector 3 (J3B1)	INTD	INTA	INTC	INTB	
PCI Bus Connector 4 (J3A2)	INTC	INTD	INTB	INTA	

NOTE

The ICH2 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 7, 9, 10, 11, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

2.8 Connectors

⚠ CAUTION

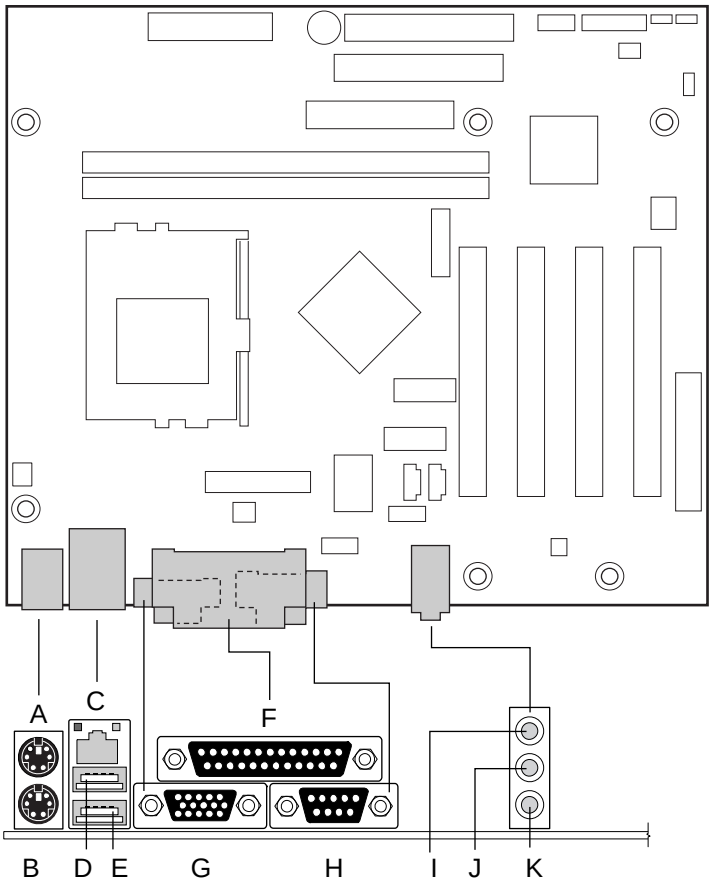
Only the back panel connectors of this D810E2CA3 board have overcurrent protection. The internal D810E2CA3 board connectors do not have overcurrent protection; they should connect only to devices inside the computer chassis, such as fans and internal peripherals. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could damage the computer, the interconnecting cable, and the external devices themselves.

This section describes the board's connectors. The connectors can be divided into the following groups.

- Back panel I/O connectors (see page 49)
  - PS/2 keyboard and mouse
  - LAN (optional)
  - USB (two)
  - VGA
  - Parallel port
  - Serial port A
  - Audio (line out, line in, and mic in)
- Internal I/O connectors (see page 53)
  - Audio (ATAPI CD-ROM, ATAPI-style auxiliary line in, front panel audio)
  - Digital video interface (optional)
  - Fans (two)
  - Power
  - Wake on LAN technology (optional)
  - Add-in boards (one CNR connector and four PCI bus connectors)
  - Diskette drive
  - IDE (two)
- External I/O connectors (see page 63)
  - Serial port B
  - Front panel USB (one connector, two ports)
  - Front panel (power/sleep/message-waiting LED, power switch, hard drive activity LED, reset switch, infrared port, and auxiliary front panel LED)

2.8.1 Back Panel Connectors

Figure 8 shows the location of the back panel connectors. The back panel connectors are color-coded in compliance with PC 99 recommendations. The figure legend below lists the colors used.



Item	Description	Color	For more information see:
A	PS/2 mouse	Green	Table 19
B	PS/2 keyboard	Purple	Table 19
C	RJ-45 LAN	Black	Table 20
D	USB port 0	Black	Table 21
E	USB port 1	Black	Table 21
F	Parallel port	Burgundy	Table 23
G	VGA port	Dark blue	Table 22
H	Serial port A	Teal	Table 24
I	Audio line in	Lime green	Table 25
J	Audio line out	Light blue	Table 26
K	Mic in	Pink	Table 27

Figure 8. Back Panel Connectors

Table 19. PS/2 Keyboard/Mouse Connectors

Pin	Signal
1	Data
2	Not connected
3	Ground
4	+5 V (fused)
5	Clock
6	Not connected

Table 20. RJ-45 LAN Connector (Optional)

Pin	Signal Name
1	TxD +
2	TxD -
3	RxD +
4	Ground
5	Ground
6	RxD -
7	Ground
8	Ground

Table 21. USB Connectors

Pin	Signal
1	+5 V (fused)
2	USBP0# [USBP1#]
3	USBP0 [USBP1]
4	Ground

Signal names in brackets ([ ]) are for USB ports 1.

Table 22. VGA Connector

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	Red	6	Ground	11	Not connected
2	Green	7	Ground	12	DDC_SDA
3	Blue	8	Ground	13	HSYNC
4	Not connected	9	+5 V (fused)	14	VSYNC
5	Ground	10	Ground	15	DDC_SCL

Table 23. Parallel Port Connector

Pin	Std Signal	ECP Signal	EPP Signal	I/O
1	STROBE#	STROBE#	WRITE#	I/O
2	PD0	PD0	PD0	I/O
3	PD1	PD1	PD1	I/O
4	PD2	PD2	PD2	I/O
5	PD3	PD3	PD3	I/O
6	PD4	PD4	PD4	I/O
7	PD5	PD5	PD5	I/O
8	PD6	PD6	PD6	I/O
9	PD7	PD7	PD7	I/O
10	ACK#	ACK#	INTR	I
11	BUSY	BUSY#, PERIPHACK	WAIT#	I
12	PERROR	PE, ACKREVERSE#	PE	I
13	SELECT	SELECT	SELECT	I
14	AUDOFD#	AUDOFD#, HOSTACK	DATASTB#	O
15	FAULT#	FAULT#, PERIPHREQST#	FAULT#	I
16	INIT#	INIT#, REVERSERQST#	RESET#	O
17	SLCTIN#	SLCTIN#	ADDRSTB#	O
18 - 25	Ground	Ground	Ground	-

Table 24. Serial Port A Connector

Pin	Signal
1	DCD (Data Carrier Detect)
2	SIN# (Serial Data In)
3	SOUT# (Serial Data Out)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request to Send)
8	CTS (Clear to Send)
9	RI (Ring Indicator)

Table 25. Audio Line Out Connector

Pin	Signal
Tip	Audio left out
Ring	Audio right out
Sleeve	Ground

Table 26. Audio Line In Connector

Pin	Signal
Tip	Audio left in
Ring	Audio right in
Sleeve	Ground

Table 27. Audio Mic In Connector

Pin	Signal
Tip	Mono in
Ring	Mic bias voltage
Sleeve	Ground

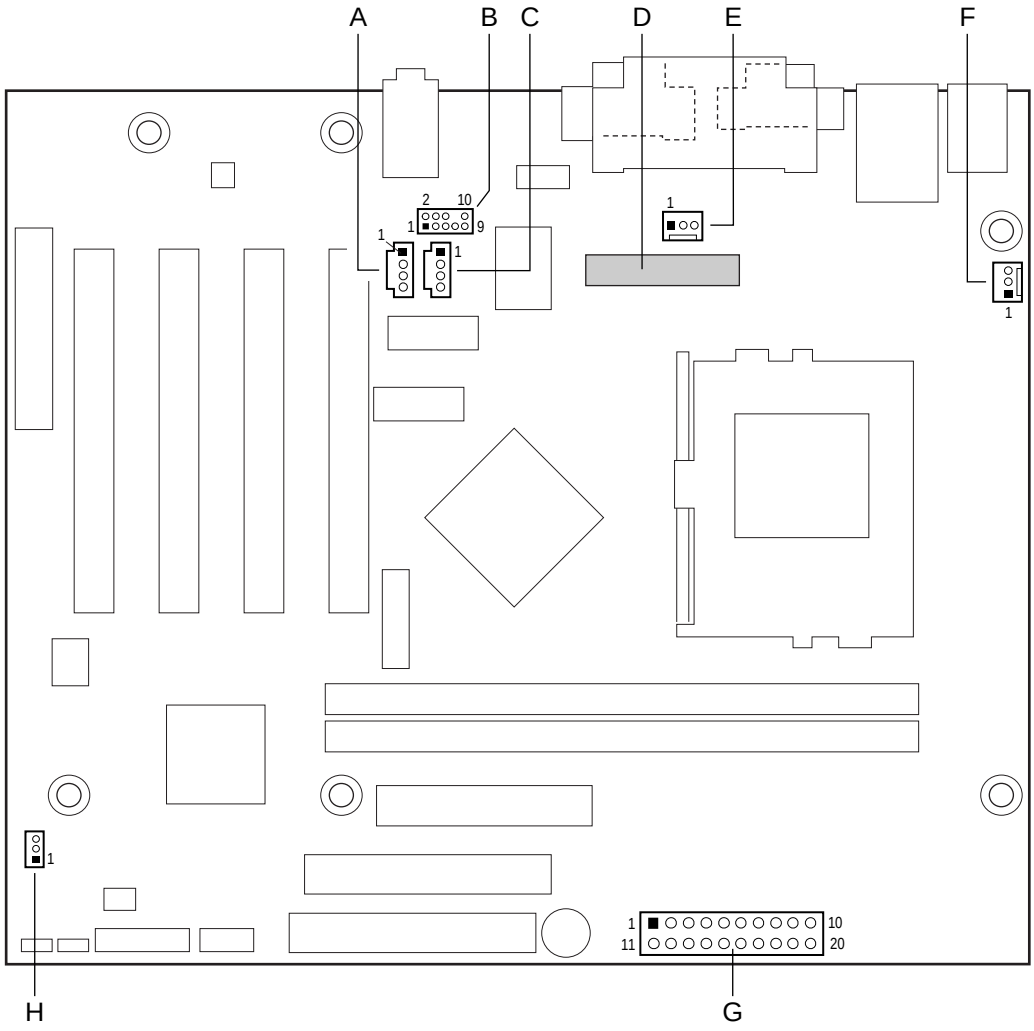
2.8.2 Internal I/O Connectors

The internal I/O connectors are divided into the following functional groups:

- Audio, video, power, and hardware control (see page 54)
  - ATAPI CD-ROM
  - Front panel audio
  - Auxiliary line in, ATAPI style
  - Digital video out (optional)
  - Fans (two)
  - Power
  - Wake on LAN technology (optional)
- Add-in boards and peripheral interfaces (see page 58)
  - CNR (communication and networking riser) (optional)
  - PCI bus (four)
  - Diskette drive
  - IDE (two)

2.8.2.1 Audio, Video, Power, and Hardware Control Connectors

Figure 9 shows the location of the audio, video, power, and hardware control connectors.



Item	Description	Reference Designator	For more information see:
A	ATAPI CD-ROM (black)	J2D1	Table 28
B	Front panel audio	J2E1	Table 29
C	Auxiliary line in, ATAPI style (white)	J2E2	Table 30
D	Digital video out (Optional)	J2G2	Table 31
E	Chassis fan (Fan 2)	J2G1	Table 32
F	Processor fan (Fan 1)	J2K1	Table 33
G	Power	J8G1	Table 34
H	Wake on LAN technology	J7A1	Table 35

Figure 9. Audio, Video, Power, and Hardware Control Connectors

Table 28. ATAPI CD-ROM Connector (J2D1)

Pin	Signal
1	Left audio input from CD-ROM
2	CD audio differential ground
3	CD audio differential ground
4	Right audio input from CD-ROM

Table 29. Front Panel Audio Connector (J2E1)

Pin	Signal Name	Pin	Signal Name
1	MICIN_FP	2	Ground
3	MIC_BIAS	4	AUD_ANALOG
5	AUD_FPOUT_R	6	AUD_RET_R
7	Reserved	8	(Pin removed)
9	AUD_FPOUT_L	10	AUD_RET_L

Table 30. Auxiliary Line In Connector (J2E2)

Pin	Signal
1	Left auxiliary line in
2	Ground
3	Ground
4	Right auxiliary line in

Table 31. Optional Digital Video Out Connector (J2G2)

Pin	Signal Name	Pin	Signal Name
1	LTVCLKIN	2	+5 V
3	P_RST_SLOTS#	4	LTVCL_3V
5	Ground	6	LTVDA_3V
7	Ground	8	LTVVSYNC
9	Ground	10	LTVHSYNC
11	Ground	12	LTVDAT0
13	Ground	14	LTVDAT1
15	Ground	16	LTVDAT2
17	Ground	18	LTVDAT3
19	Ground	20	LTVDAT4
21	Ground	22	LTVDAT5
23	Ground	24	LTVDAT6
25	Ground	26	LTVDAT7
27	Ground	28	LTVDAT8
29	Ground	30	LTVDAT9
31	Ground	32	LTVDAT10
33	Ground	34	LTVDAT11
35	Ground	36	LTVCLKOUT0
37	Ground	38	LTVCLKOUT1
39	Ground	40	LTVBLNK#

Table 32. Processor Fan Connector (J2K1)

Pin	Signal
1	Ground
2	+12 V
3	Ground

Table 33. Chassis Fan Connector (J2G1)

Pin	Signal
1	FAN_DRIVE
2	+12 V
3	Reserved

Table 34. Power Connector (J8G1)

Pin	Signal	Pin	Signal
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	PS-ON# (power supply remote on/off)
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWRGD (Power Good)	18	Reserved
9	+5 VSB	19	+5 V
10	+12 V	20	+5 V

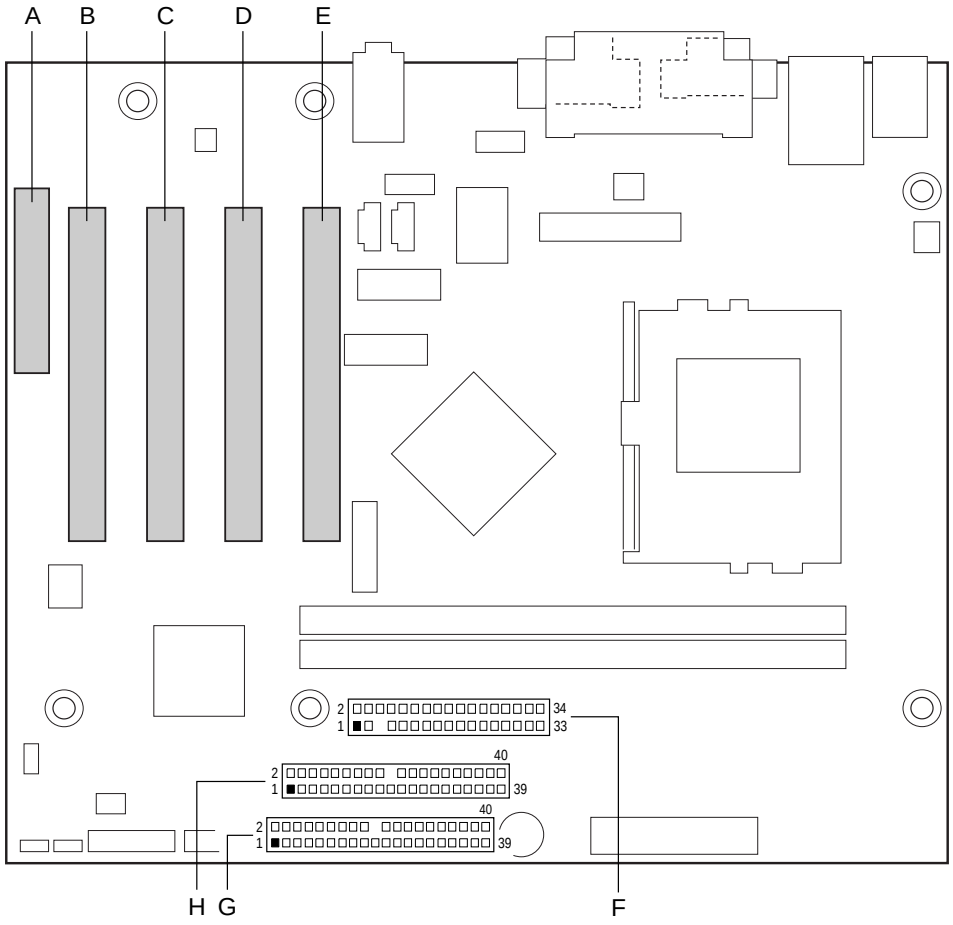
Table 35. Optional Wake on LAN Technology Connector (J7A1)

Pin	Signal
1	+5 VSB
2	Ground
3	WOL

2.8.2.2 Add-in Board and Peripheral Interface Connectors

Figure 10 shows the location of the peripheral interface connectors. Note the following considerations for the PCI bus connectors:

- All of the PCI bus connectors are bus master capable.
- PCI bus connector 2 has SMBus signals routed to it. This enables PCI bus add-in boards with SMBus support to access sensor data on the board. The specific SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40
  - The SMBus data line is connected to pin A41



Item	Description	Reference Designator	For more information see:
A	CNR (optional)	J3A1	Table 36
B	PCI bus connector 4	J3A2	Table 37
C	PCI bus connector 3	J3B1	Table 37
D	PCI bus connector 2	J3C1	Table 37
E	PCI bus connector 1	J3D1	Table 37
F	Diskette drive	J7E1	Table 38
G	Primary IDE	J8D2	Table 39
H	Secondary IDE	J8D1	Table 39

Figure 10. Add-in Board and Peripheral Interface Connectors

NOTE

PCI bus connector 1 does not physically support full-length PCI add-in boards. Use only normal-length (or smaller) PCI add-in boards in PCI bus connector 1.

Table 36. CNR Connector (J3A1)

Pin	Signal Name	Pin	Signal Name
A1	Reserved	B1	Reserved
A2	Reserved	B2	Reserved
A3	Ground	B3	Reserved
A4	Reserved	B4	Ground
A5	Reserved	B5	Reserved
A6	Ground	B6	Reserved
A7	LAN_TXD2	B7	Ground
A8	LAN_TXD0	B8	LAN_TXD1
A9	Ground	B9	LAN_RSTSYNC
A10	LAN_CLK	B10	Ground
A11	LAN_RXD1	B11	LAN_RXD2
A12	Reserved	B12	LAN_RXD0
A13	USB+	B13	Ground
A14	Ground	B14	Reserved
A15	USB-	B15	+5V (dual)
A16	+12V	B16	USB_OC
A17	Ground	B17	Ground
A18	+3.3V (dual)	B18	-12V
A19	+5VD	B19	+3.3V
A20	Ground	B20	Ground
A21	EEDI	B21	EED0
A22	EECS	B22	EECK
A23	SMB_A1	B23	Ground
A24	SMB_A2	B24	SMB_A0
A25	SMB_SDA	B25	SMB_SCL
A26	AC97_RESET	B26	CDC_DWN_ENAB
A27	Reserved	B27	Ground
A28	AC97_SDATA_IN1	B28	AC97_SYNC
A29	AC97_SDATA_IN0	B29	AC97_SDATA_OUT
A30	Ground	B30	AC97_BITCLK

For information about	Refer to
The CNR	Section 1.11, page 32

Table 37. PCI Bus Connectors (J3A2, J3B1, J3C1, J3D1)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	Ground (TRST#) (Note 1)	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	Ground (TCK) (Note 1)	A33	+3.3 V	B33	C/BE2#
A3	+5 V (TMS) (Note 1)	B3	Ground	A34	FRAME#	B34	Ground
A4	+5 V (TDI) (Note 1)	B4	Not connect ed (TDO) (Note 1)	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#
A9	Reserved	B9	Not connected (PRSNT1#) (Note 1)	A40	Reserved (Note 2)	B40	PERR#
A10	+5 V (I/O)	B10	Reserved	A41	Reserved (Note 3)	B41	+3.3 V
A11	Reserved	B11	Not connected (PRSNT2#) (Note 1)	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	+3.3 V aux	B14	Reserved	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V (I/O)	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	PME#	B19	+5 V (I/O)	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01
A28	AD22	B28	Ground	A59	+5 V (I/O)	B59	+5 V (I/O)
A29	AD20	B29	AD21	A60	REQ64C#	B60	ACK64C#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

Notes:

1. These signals (in parentheses) are optional in the PCI specification and are not currently implemented.
2. On PCI bus connector 2, this pin is connected to the optional SMBus clock line.
3. On PCI bus connector 2, this pin is connected to the optional SMBus data line.

Table 38. Diskette Drive Connector (J7E1)

Pin	Signal	Pin	Signal
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	FDINDX# (Index)
9	Ground	10	FDM00# (Motor Enable A)
11	Ground	12	Not connected
13	Ground	14	FDDS0# (Drive Select A)
15	Ground	16	Not connected
17	Not connected	18	FDDIR# (Stepper Motor Direction)
19	Ground	20	FDSTEP# (Step Pulse)
21	Ground	22	FDWD# (Write Data)
23	Ground	24	FDWE# (Write Enable)
25	Ground	26	FDTRK0# (Track 0)
27	Not connected	28	FDWPD# (Write Protect)
29	Ground	30	FDRDATA# (Read Data)
31	Ground	32	FDHEAD# (Side 1 Select)
33	Ground	34	DSKCHG# (Diskette Change)

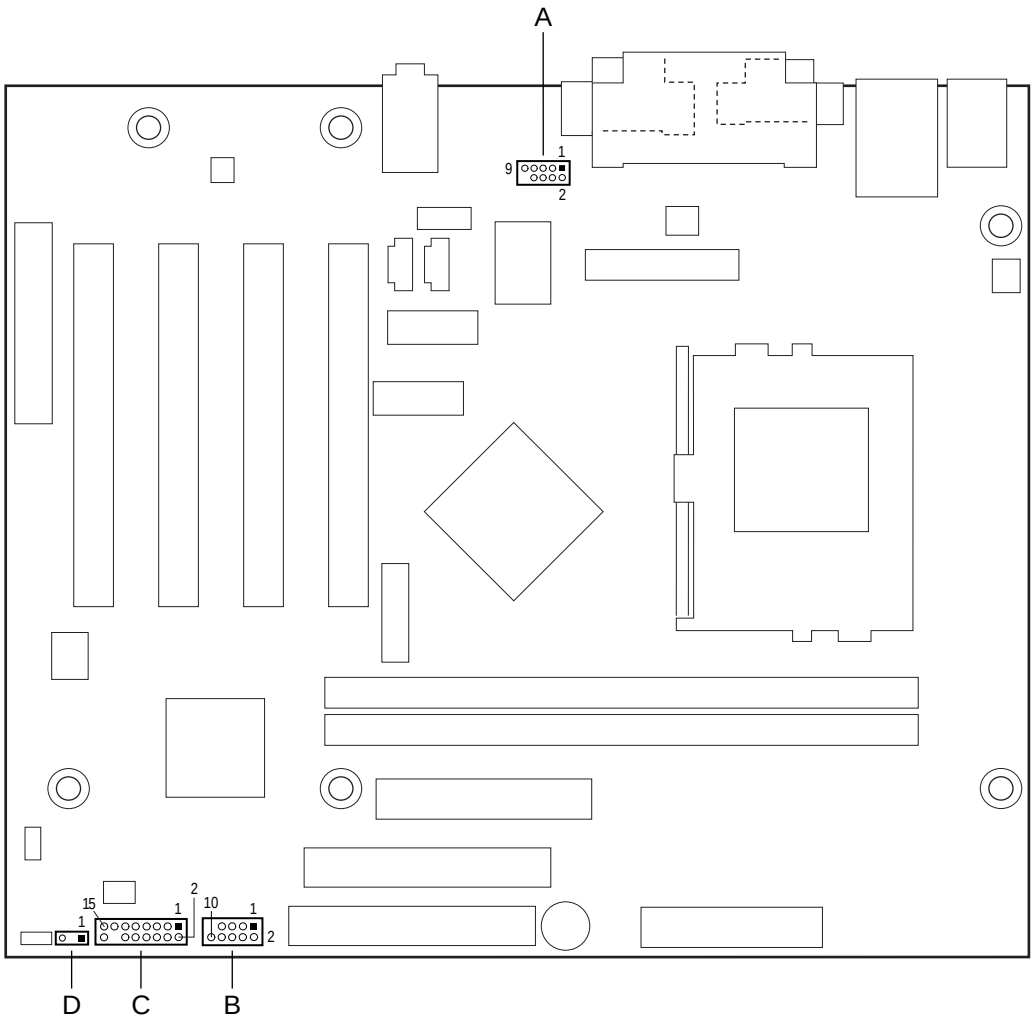
Table 39. IDE Connectors (J8D1, J8D2)

Pin	Signal	Pin	Signal
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	P_ALE (Cable Select pull-up)
29	DDACK0# [DDACK1#]	30	Ground
31	IRQ 14 [IRQ 15]	32	Reserved
33	DAG1 (Address 1)	34	Reserved
35	DAG0 (Address 0)	36	DAG2Address 2
37	Chip Select 1P# [Chip Select 1S#]	38	Chip Select 3P# [Chip Select 3S#]
39	Activity#	40	Ground

Note: Signal names in brackets ([ ]) are for the secondary IDE connector.

2.8.3 External I/O Connectors

Figure 11 shows the location of the external I/O connectors.



Item	Description	Reference Designator	For more information see:
A	Serial port B	J1E2	Table 40
B	Front panel USB	J8B1	Table 41
C	Front panel connector	J8B2	Table 43
D	Auxiliary front panel power LED	J8A3	Table 42

Figure 11. External I/O Connectors

Table 40. Serial Port B Connector (J1E2)

Pin	Signal	Pin	Signal
1	DCD (Data Carrier Detect)	2	DSR (Data Set Ready)
3	SIN# (Serial Data In)	4	RTS (Request to Send)
5	SOUT# (Serial Data Out)	6	CTS (Clear to Send)
7	DTR (Data Terminal Ready)	8	RI (Ring Indicator)
9	Ground		

Table 41. Front Panel USB Connector (J8B1)

Pin	Signal	Pin	Signal
1	V_5P0_FP_USB	2	V_5P0_FP_USB
3	I_ICH_USB_FP_P0_CONN#	4	I_ICH_USB_FP_P1_CONN#
5	I_ICH_USB_FP_P0_CONN	6	I_ICH_USB_FP_P1_CONN
7	Ground	8	Ground
9	Pin removed	10	FP_HDR_OC1_2#

2.8.3.1 Auxiliary Front Panel Power LED Connector

This connector duplicates the signals on pins 2 and 4 of the front panel connector.

Table 42. Auxiliary Front Panel Power LED Connector (J8A3)

Pin	Signal	In/Out	Description
1	HDR_BLNK_GRN	Out	Front panel green LED
2	No connect		
3	HDR_BLNK_YEL	Out	Front panel yellow LED

2.8.3.2 Front Panel Connector

This section describes the functions of the front panel connector. Table 43 lists the signal names of the front panel connector.

Table 43. Front Panel Connector (J8B2)

Pin	Signal	In/Out	Description	Pin	Signal	In/Out	Description
1	HD_PWR	Out	Hard disk LED pull-up (330 Ω) to +5 V	2	HDR_BLNK_GRN	Out	Front panel green LED
3	HDA#	Out	Hard disk active LED	4	HDR_BLNK_YEL	Out	Front panel yellow LED
5	GND		Ground	6	FPBUT_IN	In	Power switch
7	FP_RESET#	In	Reset switch	8	GND		Ground
9	+5 V	Out	Power	10	N/C		
11	Reserved		Reserved	12	GND		Ground
13	GND		Ground	14	(pin removed)		Not connected
15	Reserved		Reserved	16	+5 V	Out	Power

2.8.3.2.1 Reset Switch Connector

Pins 5 and 7 can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the D810E2CA3 board resets and runs the POST.

2.8.3.2.2 Hard Drive Activity LED Connector

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. For the LED to function properly, an IDE drive must be connected to the onboard IDE interface.

2.8.3.2.3 Power/Sleep/Message Waiting LED Connector

Pins 2 and 4 can be connected to a single- or dual-colored LED. Table 44 shows the possible states for a single-colored LED. Table 45 shows the possible states for a dual-colored LED.

Table 44. States for a Single-colored Power LED

LED State	Description	ACPI State
Off	Off	S1, S3, S5
Steady Green	Running	S0
Blinking Green	Running / message waiting	S0

Table 45. States for a Dual-colored Power LED

LED State	Description	ACPI State
Off	Off	S5
Steady Green	Running	S0
Blinking Green	Running / message waiting	S0
Steady Yellow	Sleeping	S1, S3
Blinking Yellow	Sleeping / message waiting	S1, S3

NOTE

To use the message waiting function, ACPI must be enabled in the operating system and a message-capturing application must be invoked.

2.8.3.3 Power Switch Connector

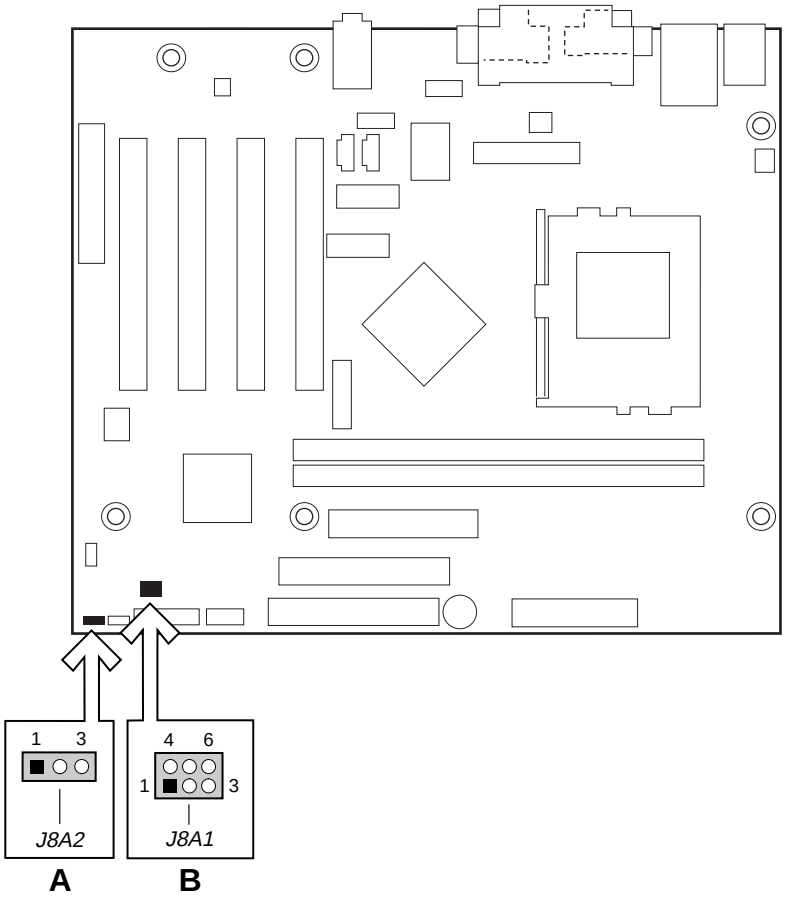
Pins 6 and 8 can be connected to a front panel power switch. The switch must pull pin 6 to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the board.) At least two seconds must pass before the power supply will recognize another on/off signal.

2.9 Jumper Blocks

CAUTION

Do not move the jumper with the power on. Always turn off the power and unplug the power cord from the computer before changing the jumper. Otherwise, the board could be damaged.

Figure 12 shows the location of the board's jumper blocks.



A BIOS setup configuration jumper block
B USB port 0 configuration jumper

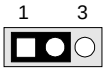
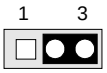
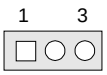
Figure 12. Location of the Jumper Blocks

2.9.1 BIOS Setup Configuration Jumper Block

This 3-pin jumper block determines the BIOS Setup program's mode. Table 46 describes the jumper settings for the three modes: normal, configure, and recovery.

When the jumper is set to configuration mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

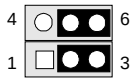
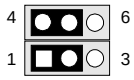
Table 46. BIOS Setup Configuration Jumper Settings

Function / Mode	Jumper Setting	Configuration
Normal	1-2 	The BIOS uses current configuration information and passwords for booting.
Configure	2-3 	After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	None 	The BIOS attempts to recover the BIOS configuration. A recovery medium is required.

2.9.2 USB Port 0 Configuration Jumper Block

This 6-pin jumper block allows rerouting of USB Port 0 signals. Table 47 describes the jumper settings.

Table 47. USB Port 0 Configuration Jumper Settings

Jumper Setting	Configuration
2-3 and 5-6 	USB Port 0 signals are routed for a front panel USB connector.
1-2 and 4-5 	USB Port 0 signals are routed to the CNR connector.

2.10 Mechanical Considerations

2.10.1 Form Factor

The D810E2CA3 board is designed to fit into a microATX or a standard ATX-form-factor chassis. Figure 13 illustrates the mechanical form factor for the board. Dimensions are given in inches [millimeters]. The outer dimensions are 9.60 inches by 8.00 inches [243.84 x 203.20 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the microATX specification (see Section 1.3).

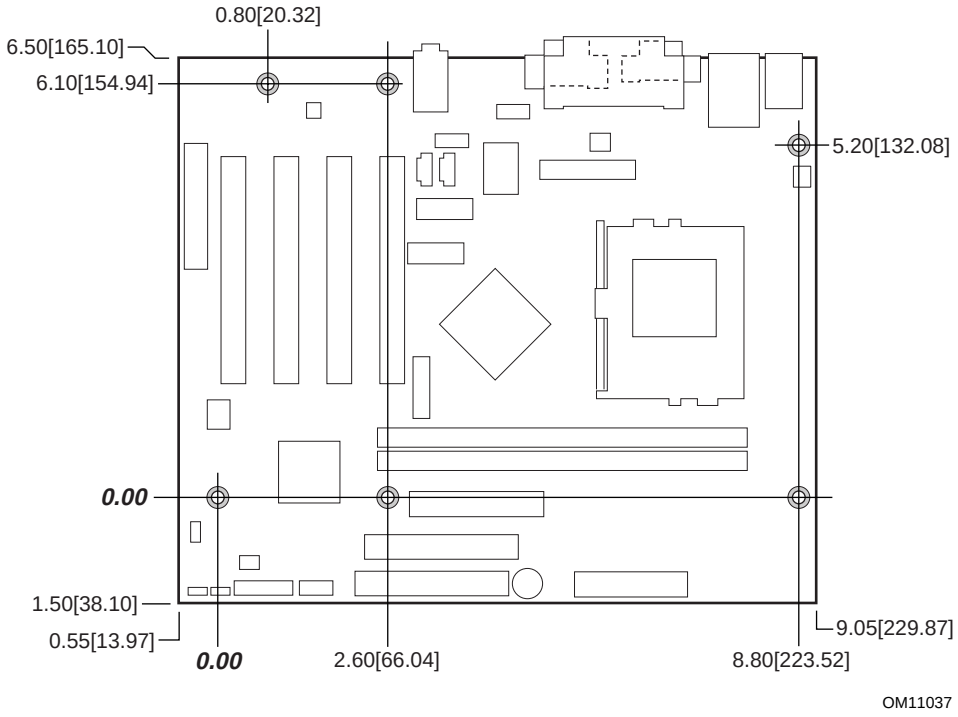


Figure 13. Board Dimensions

2.10.2 I/O Shield

The back panel I/O shield for the board must meet specific dimension and material requirements. Systems based on this board need the back panel I/O shield to pass emissions (EMI) certification testing. Figure 14 shows the critical dimensions of the chassis-independent I/O shield. Dimensions are given in inches and [millimeters]. The figure indicates the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the microATX specification.

NOTE

A chassis-independent I/O shield designed to be compliant with the microATX chassis specification is available from Intel. The actual punchouts may differ depending on the board manufacturing options.

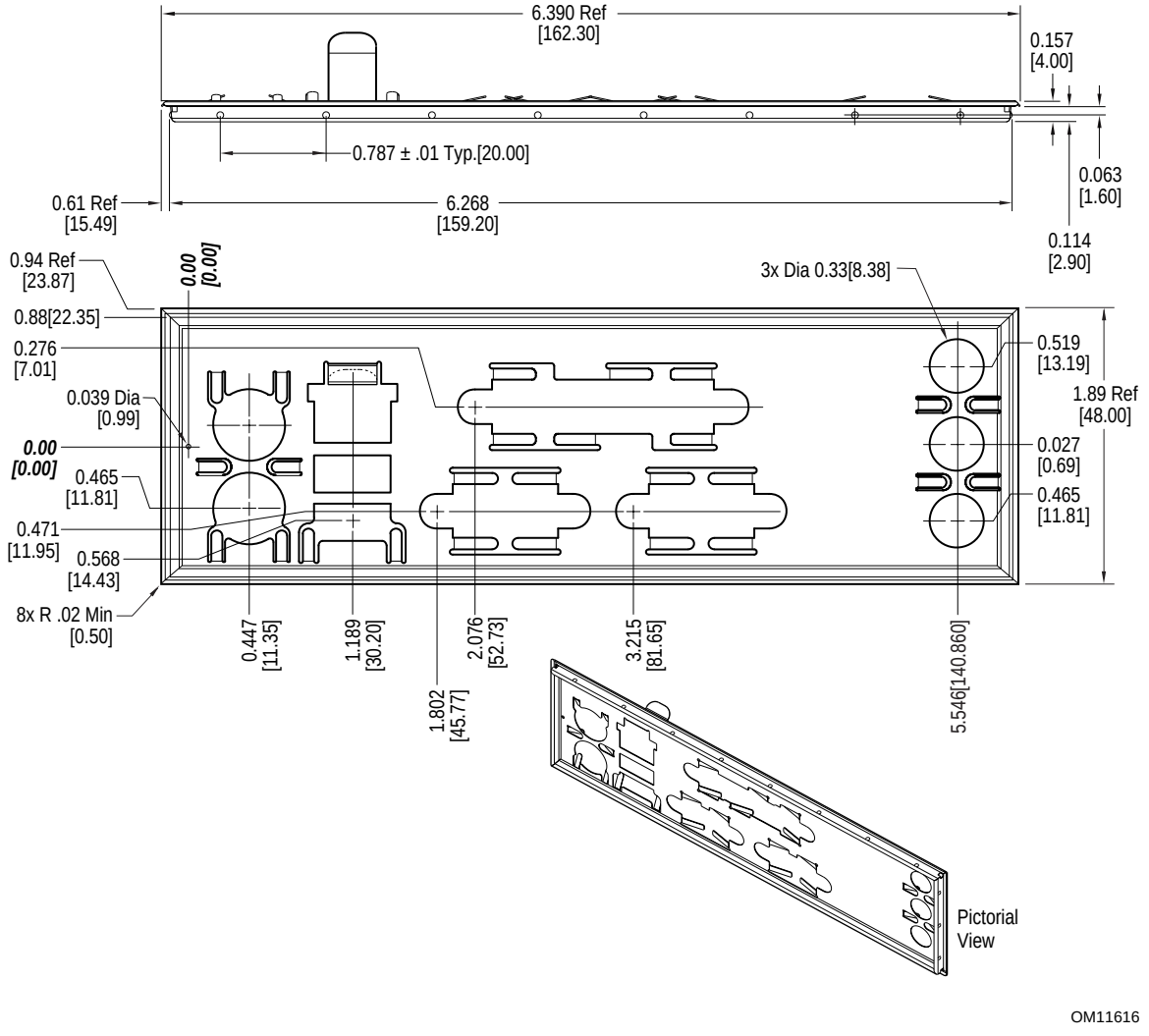


Figure 14. Back Panel I/O Shield Dimensions

2.11 Electrical Considerations

2.11.1 Power Consumption

Table 48 lists typical power usage measurements. These figures are provided to assist in selecting appropriate desktop power supplies for the D810E2CA3 board. Power usage measurements will vary depending upon actual system configurations.

The power measurements listed in Table 48 were made with a desktop computer containing the D810E2CA3 board and the following:

- 1.0B GHz Intel Pentium III processor with a 256 KB cache
- 256 MB SDRAM
- 3.5-inch diskette drive
- 8.4 GB IDE hard disk drive
- IDE CD-ROM drive
- IDE DVD drive

This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows 98 desktop mode are measured at 640 x 480 x 256 colors and 60 Hz refresh rate. AC watts are measured with a typical 200 W supply, nominal input voltage and frequency, with a true RMS wattmeter at the line input.

NOTE

Actual system power consumption depends upon system configuration. The power supply should comply with the recommendations found in the ATX form factor specification.

Table 48. Power Usage

		DC Current at:				
Mode	**AC Power**	**+3.3 V**	**+5 V**	**+12 V**	**-12 V**	**+5 VSB**
Windows 98 ACPI S0	57 W	1.60 A	2.68 A	0.30 A	0.02 A	0.07 A
Windows 98 ACPI S1	25 W	1.04 A	0.54 A	0.31 A	0.02 A	0.07 A
Windows 98 ACPI S3	4 W	0.0 A	0.0 A	0.0 A	0.0 A	0.0 A
Windows 98 ACPI S5	4 W	0.0 A	0.0 A	0.0 A	0.0 A	0.069 A
Windows 98 SE APM Full On	62 W	1.29 A	4.38 A	0.254 A	0.029 A	0.065 A
Windows 98 SE APM Suspend (Start menu/Standby)	29 W	1.15 A	0.592 A	0.231 A	0.029 A	0.065 A

2.11.2 Add-in Board Considerations

The board is designed to provide 2 A (average) of +5 V current for each add-in board. The total +5 V current draw for add-in boards in a fully-loaded board (all four expansion slots filled) must not exceed 8 A.

2.11.3 Standby Current Requirements

⚠ CAUTION

If the standby current necessary to support multiple wake events from the PCI and/or USB buses exceeds power supply capacity, the D810E2CA3 board may lose register settings stored in memory, etc. Calculate the standby current requirements using the steps described below.

Power supplies used with the D810E2CA3 board must be able to provide enough standby current to support the Instantly Available (ACPI S3 sleep state) configuration as outlined in Table 49.

Values are determined by specifications such as PCI 2.2. Actual measured values may vary.

To estimate the amount of standby current required for a particular system configuration, standby current requirements of all installed components must be added to determine the total standby current requirement. Refer to the descriptions in Table 49 and review the following steps:

1. Note the total D810E2CA3 desktop board standby current requirement.
2. Add the PCI 2.2 slots with wake enabled devices installed and multiply by the standby current requirement for wake enabled devices.
3. Add the PCI 2.2 slots with wake enabled devices installed, and multiply by the standby current requirement for non-wake enabled devices.
4. Add all additional wake enabled devices' and non-wake enabled devices' standby current requirements as applicable.
5. Add all the required current totals from steps 1 through 4 to determine the total estimated standby current power supply requirement.

Table 49. Standby Current Requirements

Instantly Available Current Support (Estimated for integrated board components)	Description	Standby Current Requirements (mA)
	Total for the D810E2CA3 board	228 mA (with onboard LAN)
Instantly Available Stand-by Current Support • **Estimated for add-on components** • **Add to Instantly Available total current requirement** **(See instructions above)**	PCI 2.2 slots (wake enabled)	117 mA
	PCI 2.2 slots (non-wake enabled)	101 mA
	Wake on LAN technology connector	137 mA

NOTE

IBM PS/2 Port Specification (Sept 1991) states

- *275 mA for keyboard*
- *70 mA for the mouse (not wake-enable device)*

PCI requirements are calculated by totaling the following:

- *One wake-enabled device @ 375 mA*
- *Non wake-enabled devices @ 20 mA each*

2.11.4 Fan Power Requirements

Table 50 lists the maximum DC voltage and current requirements for the fans when the board is in sleep mode or normal operating mode. Power consumption is independent of the operating system used and other variables.

Table 50. Fan DC Power Requirements

Fan Type	Mode	Voltage	Maximum Current (Amps)
Chassis (J2G1)	Sleep	0 VDC	0 mA
	Normal	+ 12 VDC	90 mA (current limited) (Note)
Processor (J2K1)	Sleep	0 VDC	0 mA
	Normal	+ 12 VDC	250 mA (current limited) (Note)

Note: Maximum current value is dependent on the fan and the fan's RPM rating.

For information about	Refer to
The location of the fan connectors	Figure 9, page 54
The signal names of the processor fan connector	Table 32, page 56
The signal names of the chassis fan connector	Table 33, page 56

2.11.5 Power Supply Considerations

⚠ CAUTION

The 5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options. Refer to Section 2.11.3 on page 71 for additional information.

System integrators should refer to the power usage values listed in Table 48 when selecting a power supply for use with this board. The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.2.2)
- All timing parameters (Section 4.2.2.3)
- All voltage tolerances (Section 4.2.3)

For information about	Refer to
The ATX form factor specification	Section 1.3, page 16

2.12 Thermal Considerations

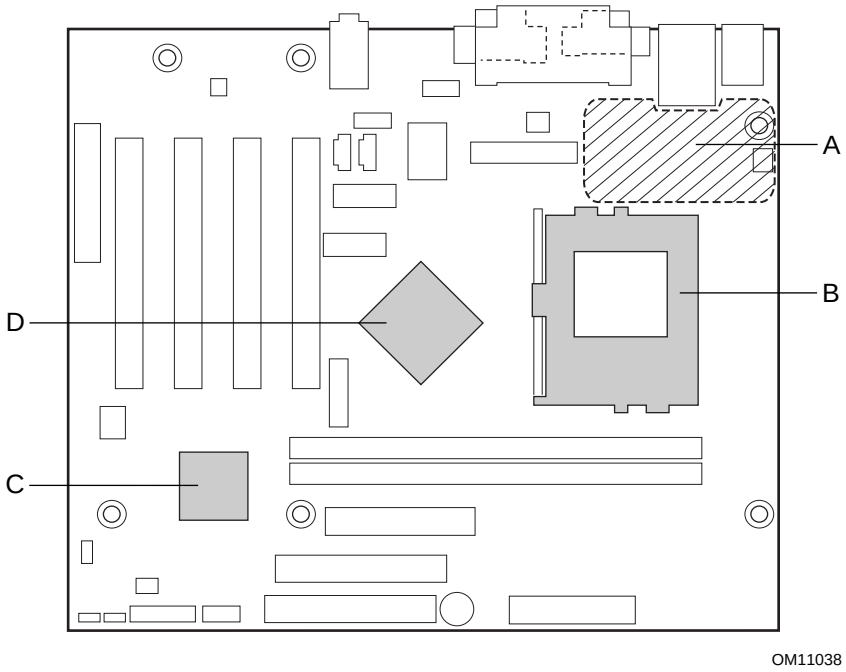
CAUTION

An ambient temperature that exceeds the board's maximum operating temperature by 10 °C could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.14.

CAUTION

The processor voltage regulator area (item A in Figure 15) can reach a temperature of up to 85 °C in an open chassis. System integrators should ensure that proper airflow is maintained in the voltage regulator circuit. Failure to do so may result in damage to the voltage regulator circuit.

Figure 15 shows the locations of the localized high temperature zones.



A	Processor
B	Voltage regulator area
C	Intel 82801BA ICH2
D	Intel 82810E GMCH

Figure 15. High-Temperature Zones

Table 51 provides maximum component case temperatures for board components that could be sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the board.

Table 51. Thermal Considerations for Components

Component	Maximum Case Temperature
Intel Pentium III processor	For processor case temperature, see processor datasheets and processor specification updates
Intel Celeron processor	
Intel 82810E DC-133 GMCH	70 °C (under bias)
Intel 82801BA ICH2	109 °C (under bias)

For information about	Refer to
Intel Pentium III processor datasheets and specification updates	Section 1.2, page 16
Intel Celeron processor datasheets and specification updates	Section 1.2, page 16

2.13 Reliability

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is for estimating repair rates and spare parts requirements.

The Mean Time Between Failures (MTBF) data is calculated from predicted data at 35 ºC.

Board MTBF: 377,018 hours

2.14 Environmental Specifications

Table 52. Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	30 g trapezoidal waveform		
	Velocity change of 170 inches/second		
Packaged	Half sine 2 millisecond		
	Product Weight (pounds)	Free Fall (inches)	Velocity Change (inches/sec)
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz: 0.01 g^2 Hz sloping up to 0.02 g^2 Hz		
	20 Hz to 500 Hz: 0.02 g^2 Hz (flat)		
Packaged	10 Hz to 40 Hz: 0.015 g^2 Hz (flat)		
	40 Hz to 500 Hz: 0.015 g^2 Hz sloping down to 0.00015 g^2 Hz		

2.15 Regulatory Compliance

This section describes the D810E2CA3 board's compliance with U.S. and international safety and electromagnetic compatibility (EMC) regulations.

2.15.1 Safety Regulations

Table 53 lists the safety regulations the D810E2CA3 board complies with when correctly installed in a compatible host system.

Table 53. Safety Regulations

Regulation	Title
UL 1950/CSA C22.2 No. 950, 3rd edition	Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
EN 60950, 2nd Edition, 1992 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)
IEC 60950, 2nd Edition, 1991 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)
EMKO-TSE (74-SEC) 207/94	Summary of Nordic deviations to EN 60950. (Norway, Sweden, Denmark, and Finland)

2.15.2 EMC Regulations

Table 54 lists the EMC regulations the D810E2CA3 board complies with when correctly installed in a compatible host system.

Table 54. EMC Regulations

Regulation	Title
FCC (Class B)	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, Radiofrequency Devices. (USA)
ICES-003 (Class B)	Interference-Causing Equipment Standard, Digital Apparatus (Canada)
EN55022: 1994 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (European Union)
EN55024: 1998	Information Technology Equipment – Immunity Characteristics Limits and methods of measurement. (European Union)
AS/NZS 3548 (Class B)	Australian Communications Authority, Standard for Electromagnetic Compatibility. (Australia and New Zealand)
CISPR 22, 2nd Edition (Class B)	Limits and methods of measurement of Radio Disturbance Characteristics of Information Technology Equipment. (International)
CISPR 24: 1997	Information Technology Equipment – Immunity Characteristics – Limits and Methods of Measurements. (International)

2.15.3 Product Certification Markings (Board Level)

The D810E2CA3 desktop board has the following product certification markings:

- UL joint US/Canada Recognized Component mark: Consists of small c followed by a stylized backward UR and followed by a small US. Includes adjacent UL file number for Intel desktop boards: E210882 (component side).
- FCC Declaration of Conformity logo mark for Class B equipment; to include Intel name and D810E2CA3 model designation (solder side).
- CE mark: Declaring compliance to European Union (EU) EMC directive (89/336/EEC) and Low Voltage directive (73/23/EEC) (component side). The CE mark should also be on the shipping container.
- Australian Communications Authority (ACA) C-Tick mark: consists of a stylized C overlaid with a check (tick) mark (component side), followed by Intel supplier code number, N-232. The C-tick mark should also be on the shipping container.
- Printed wiring board manufacturer's recognition mark: consists of a unique UL recognized manufacturer's logo, along with a flammability rating (94V-0) (solder side).
- PB part number: Intel bare circuit board part number (solder side) A31329-001. Also includes SKU number starting with AA followed by additional alphanumeric characters.
- Battery "+ Side Up" marking: located on the component side of the board in close proximity to the battery holder.

3 Overview of BIOS Features

What This Chapter Contains

3.1 Introduction

The D810E2CA3 board uses an Intel/AMI BIOS, which is stored in flash memory and can be updated using a disk-based program. In addition to the BIOS, the flash memory contains the BIOS Setup program, POST, APM, ACPI, PCI auto-configuration utility, and Windows 98-ready Plug and Play.

This board supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOS is identified as CA81030A.86A.

For information about	Refer to
The D810E2CA3 board's compliance level with APM, ACPI, and Plug and Play	Section 1.3, page 16

3.2 BIOS Flash Memory Organization

The SST 49LF004A Firmware Hub (FWH) includes a 4 Mbit (512 KB) symmetrical flash memory device. Internally, the device is grouped into eight 64-KB blocks that are individually erasable, lockable, and unlockable.

3.3 Resource Configuration

3.3.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be onboard or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card. Autoconfiguration information is stored in ESCD format.

For information about the versions of PCI and Plug and Play supported by the BIOS, see Section 1.3.

3.3.2 IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the two IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to ATA-100 and recognizes any ATAPI compliant devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 1.3 for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66/100 features the following items are required:

- An ATA-66/100 peripheral device
- An ATA-66/100 compatible cable
- ATA-66/100 operating system device drivers

NOTE

ATA-66/100 compatible cables are backward compatible with drives using slower IDE transfer protocols. If an ATA-66/100 disk drive and a disk drive using any other IDE transfer protocol are attached to the same cable, the maximum transfer rate between the drives is reduced to that of the slowest device.

NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the management information format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system

administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

For information about	Refer to
The D810E2CA3 board's compliance level with SMBIOS	Section 1.3, page 16

3.5 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

NOTE

Legacy USB support is for keyboards, mice, and hubs only. Other USB devices are not supported in legacy mode.

3.6 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS Update utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a 1.44 MB diskette, or a CD-ROM, or from the file location on the Web.
- Intel® Flash Memory Update Utility, which requires creation of a boot diskette and manual rebooting of the system. Using this utility, the BIOS can be updated from a file on a 1.44 MB diskette (from a legacy diskette drive or an LS-120 diskette drive) or a CD-ROM.

Both utilities support the following BIOS maintenance functions:

- Verifying that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.
- Updating both the BIOS boot block and the main BIOS. This process is fault tolerant to prevent boot block corruption.
- Updating the BIOS boot block separately.
- Changing the language section of the BIOS.
- Updating replaceable BIOS modules, such as the video BIOS module.
- Inserting a custom splash screen.

NOTE

Review the instructions distributed with the upgrade utility before attempting a BIOS update.

For information about	Refer to
The Intel World Wide Web site	Section 1.2, page 16

3.6.1 Language Support

The BIOS Setup program and help messages are supported in five languages: US English, German, Italian, French, and Spanish. The default language is US English, which is present unless another language is selected in the BIOS Setup program.

3.6.2 Custom Splash Screen

During POST, an Intel splash screen is displayed by default. This splash screen can be replaced with a custom splash screen. A utility is available from Intel to assist with creating a custom splash screen. The custom splash screen can be programmed into the flash memory using the BIOS upgrade utility. Information about this capability is available on the Intel Support World Wide Web site.

For information about	Refer to
The Intel World Wide Web site	Section 1.2, page 16

3.7 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode. When recovering the BIOS, be aware of the following:

- Because of the small amount of code available in the non-erasable boot block area, there is no video support. You can only monitor this procedure by listening to the speaker or looking at the diskette drive LED.
- The recovery process may take several minutes; larger BIOS flash memory devices require more time.
- Two beeps and the end of activity in the diskette drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery.

To create a BIOS recovery diskette, a bootable diskette must be created and the BIOS update files copied to it. BIOS upgrades and the Intel Flash Memory Update Utility are available from Intel Customer Support through the Intel World Wide Web site.

⟹ NOTE

Even if the computer is configured to boot from an LS-120 diskette (in the Setup program's Removable Devices submenu), the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.

For information about	Refer to
The BIOS recovery mode jumper settings	Table 46, page 67
The Boot menu in the BIOS Setup program	Section 4.7, page 101
Contacting Intel customer support	Section 1.2, page 16

3.8 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network. The default setting is for the diskette drive to be the first boot device, the hard drive second, and the ATAPI CD-ROM third. The fourth device is disabled.

3.8.1 CD-ROM and Network Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the CD-ROM drive, the system will attempt to boot to the next defined drive.

The network can be selected as a boot device. This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed.

For information about	Refer to
The El Torito specification	Section 1.3, page 16

3.8.2 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

3.9 Fast Booting Systems with Intel® Rapid BIOS Boot

Three factors affect system boot speed:

- Selecting and configuring peripherals properly
- Using an optimized BIOS, such as the Intel® Rapid BIOS
- Selecting a compatible operating system

3.9.1 Peripheral Selection and Configuration

The following techniques help improve system boot speed:

- Choose a hard drive with parameters such as “power-up to data ready” less than eight seconds, that minimize hard drive startup delays.
- Select a CD-ROM drive with a fast initialization rate. This rate can influence POST execution time.
- Eliminate unnecessary add-in adapter features, such as logo displays, screen repaints, or mode changes in POST. These features may add time to the boot process.
- Try different monitors. Some monitors initialize and communicate with the BIOS more quickly, which enables the system to boot more quickly.

3.9.2 Intel Rapid BIOS Boot

Use of the following BIOS Setup program settings reduces the POST execution time.

In the Boot Menu:

- Set the hard disk drive as the first boot device. As a result, the POST does not first seek a diskette drive, which saves about one second from the POST execution time.
- Disable Quiet Boot, which eliminates display of the logo splash screen. This could save several seconds of painting complex graphic images and changing video modes.
- Enabled Intel Rapid BIOS Boot. This feature bypasses memory count and the search for a diskette drive

In the Peripheral Configuration submenu, disable the LAN device if it will not be used. This can reduce up to four seconds of option ROM boot time.

NOTE

It is possible to optimize the boot process to the point where the system boots so quickly that the Intel logo screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen.

This boot time may be so fast that some drives might be not be initialized at all. If this condition should occur, it is possible to introduce a programmable delay ranging from 3 to 30 seconds (using the Hard Disk Pre-Delay feature of the Advanced Menu in the IDE Configuration Submenu of the BIOS Setup Program).

For information about	Refer to
IDE Configuration Submenu in the BIOS Setup Program	Section 4.4.4, page 94

3.9.3 Operating System

The Microsoft Windows Millennium Edition (Windows Me) operating system has built-in capabilities for making PCs boot more quickly. To speed operating system availability at boot time, limit the number of applications that load into the system tray or the task bar.

3.10 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 55 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 55. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options (Note)	Can change all options (Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

Note: If no password is set, any user can change all Setup options.

For information about	Refer to
Setting user and supervisor passwords	Section 4.5, page 99

4 BIOS Setup Program

What This Chapter Contains

4.1 Introduction

The BIOS Setup program is used for viewing and changing the BIOS settings for a computer. The user accesses the BIOS Setup program by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

Maintenance	Main	Advanced	Security	Power	Boot	Exit

Table 56 lists the BIOS Setup program menu functions.

Table 56. BIOS Setup Program Menu Bar

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords and enables extended configuration mode	Allocates resources for hardware components	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features	Selects boot options and power supply controls	Saves or discards changes to Setup program options

NOTE

In this chapter, all examples of the BIOS Setup Program menu bar include the maintenance menu; however, the maintenance menu is displayed only when the board is in configuration mode. Section 2.9.1 on page 67 tells how to put the board in configuration mode.

Table 57 shows the function keys available for menu screens.

Table 57. Setup Function Keys

Setup Key	Description
<←> or <→>	Selects a different menu screen
<↑> or <↓>	Selects an item
<Tab>	Selects a field
<Enter>	Executes command or selects the submenu
<F9>	Loads the default configuration values for the current menu
<F10>	Saves the current values and exits the BIOS Setup program
<Esc>	Exits the menu

4.2 Maintenance Menu

To access this menu, select Maintenance on the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	Boot	Exit

The menu shown in Table 58 is for clearing Setup passwords and enabling extended configuration mode. Setup only displays this menu in configuration mode. See Section 2.9.1 on page 67 for configuration mode setting information.

Table 58. Maintenance Menu

Feature	Options	Description
▸ Clear All Passwords	• **Yes (default)** • No	Selecting *Yes* clears all passwords.
▸ Clear BIS Credentials	• **Yes (default)** • No	Selecting *Yes* clears the WfM BIS (Boot Integrity Service) credentials.
▸ Extended Configuration	• **Default (default)** • User-Defined	Selecting *User-Defined* allows setting memory configuration.
CPU Information		
CPU Microcode Update Revision	No options	Displays the revision number of the processor microcode.
CPU Stepping Signature	No options	Displays the processor stepping signature.

4.2.1 Extended Configuration Submenu

To access this submenu, select Maintenance on the menu bar, then Extended Configuration.

Maintenance	Main	Advanced	Security	Power	Boot	Exit

The submenu represented by Table 59 is used to set video memory cache mode. This submenu becomes available when User Defined is selected under Extended Configuration.

⚠ CAUTION

Choosing the wrong settings could cause system problems. Do not change these settings unless you have all the necessary information about the installed memory.

Table 59. Extended Configuration Menu

Feature	Options	Description
Extended Configuration	• **Default (default)** • User Defined	Enables access to the extended memory configuration options. Note: If *User-Defined* is selected, the status will be displayed in the Advanced Menu as: "Extended Menu: Used."
Memory Control		
SDRAM Auto-Configuration	• **Auto (default)** • User Defined	Sets extended memory configuration options to auto or user defined.
SDRAM CAS# Latency	• 3 • 2 • **Auto (default)**	Selects the number of clock cycles required to address a column in memory.
SDRAM RAS# to CAS# Delay	• 3 • 2 • **Auto (default)**	Selects the number of clock cycles between addressing a row and addressing a column.
SDRAM RAS# Precharge	• 3 • 2 • **Auto (default)**	Selects the length of time required before accessing a new row.

4.3 Main Menu

To access this menu, select Main on the menu bar at the top of the screen.

Maintenance	**Main**	Advanced	Security	Power	Boot	Exit

Table 60 describes the Main Menu. This menu reports processor and memory information and is used to configure the system date and system time.

Table 60. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS.
Processor Type	No options	Displays processor type.
Processor Speed	No options	Displays processor speed.
System Bus Frequency	No options	Displays the system bus frequency.
Cache RAM	No options	Displays the size of second-level cache.
Total Memory	No options	Displays the total amount of RAM on the board.
Bank 0 Bank 1	No options	Displays the type of DIMM installed in each memory bank.
Language	• **English (default)** • Espanol • Deutsch	Selects the current default language used by the BIOS.
Processor Serial Number	• **Disabled (default)** • Enabled	Enables and disables the processor serial number (only available with a Pentium III processor installed).
System Time	Hour, minute, and second	Specifies the current time.
System Date	Day of the week, month, day, and year	Specifies the current date.

4.4 Advanced Menu

To access this menu, select Advanced on the menu bar at the top of the screen.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Extended Configuration
PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

Table 61 describes the Advanced Menu. This menu is used to set advanced features that are available through the chipset.

Table 61. Advanced Menu

Feature	Options	Description
Extended Configuration	No options	Indicates whether extended configuration settings have been modified from the default setting.
PCI Configuration	No options	Allows access to PCI IRQ mapping.
Boot Configuration	No options	Configures Plug and Play and the Numlock key, and resets configuration data. When selected, displays the Boot Settings Configuration submenu.
Peripheral Configuration	No options	Configures peripheral ports and devices. When selected, displays the Peripheral Configuration submenu.
IDE Configuration	No options	Specifies type of connected IDE device.
Diskette Configuration	No options	When selected, displays the Floppy Options submenu.
Event Log Configuration	No options	Configures Event Logging. When selected, displays the Event Log Configuration submenu.
Video Configuration	No options	Configures video features. When selected, displays the Video Configuration submenu.

4.4.1 PCI Configuration Submenu

To access this submenu, select Advanced on the menu bar, then PCI Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Extended Configuration
PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 62 is used to configure the IRQ priority of PCI slots individually.

Table 62. PCI Configuration Submenu

Feature	Options	Description
PCI Slot1 IRQ Priority	• **Auto (default)** • 9 • 10 • 11	Allows the user to map the PCI IRQ for slot 1 to a particular hardware interrupt.
PCI Slot2 IRQ Priority	• **Auto (default)** • 9 • 10 • 11	Allows the user to map the PCI IRQ for slot 2 to a particular hardware interrupt.
PCI Slot3 IRQ Priority	• **Auto (default)** • 9 • 10 • 11	Allows the user to map the PCI IRQ for slot 3 to a particular hardware interrupt.
PCI Slot4 IRQ Priority	• **Auto (default)** • 9 • 10 • 11	Allows the user to map the PCI IRQ for slot 4 to a particular hardware interrupt.

4.4.2 Boot Configuration Submenu

To access this submenu, select Advanced on the menu bar, then Boot Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Extended Configuration
PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 63 is used to set Plug and Play options, resetting configuration data, and the power-on state of the Numlock key.

Table 63. Boot Setting Configuration Submenu

Feature	Options	Description
Plug & Play O/S	• **No (default)** • Yes	Specifies if manual configuration is desired. *No* lets the BIOS configure all devices. This setting is appropriate when using a Plug and Play operating system. *Yes* lets the operating system configure Plug and Play devices. This option is available for use during lab testing.
Reset Config Data	• **No (default)** • Yes	Clears the BIOS configuration data on the next boot.
Numlock	• Off • **On (default)**	Specifies the power on state of the Numlock feature on the numeric keypad of the keyboard.

4.4.3 Peripheral Configuration Submenu

To access this submenu, select Advanced on the menu bar, then Peripheral Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Extended Configuration
PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 64 is used to configure computer peripherals.

Table 64. Peripheral Configuration Submenu

Feature	Options	Description
Serial port A	• Disabled • Enabled • **Auto (default)**	Configures serial port A. *Auto* assigns the first free COM port, normally COM1, the address 3F8h, and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Base I/O address	• **3F8 (default)** • 2F8 • 3E8 • 2E8	Specifies the base I/O address for serial port A, if Serial Port A is set to Enabled.
Interrupt	• IRQ 3 • **IRQ 4 (default)**	Specifies the interrupt for serial port A, if Serial Port A is set to Enabled.
Serial port B	• Disabled • Enabled • **Auto (default)**	Configures serial port B. *Auto* assigns the first free COM port, normally COM2, the address 2F8h and the interrupt IRQ3. An * (asterisk) displayed next to an address indicates a conflict with another device. If either serial port address is set, that address will not appear in the list of options for the other serial port.
Base I/O address	• **2F8 (default)** • 3E8 • 2E8	Specifies the base I/O address for serial port B.
Interrupt	• **IRQ 3 (default)** • IRQ 4	Specifies the interrupt for serial port B.

continued

Table 64. Peripheral Configuration Submenu (continued)

Feature	Options	Description
Parallel port	• Disabled • Enabled • **Auto (default)**	Configures the parallel port. *Auto* assigns LPT1 the address 378h and the interrupt IRQ7. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	• Output Only • **Bi-directional (default)** • EPP • ECP	Selects the mode for the parallel port. Not available if the parallel port is disabled. *Output Only* operates in AT†-compatible mode. *Bi-directional* operates in PS/2-compatible mode. *EPP* is Extended Parallel Port mode, a high-speed bi-directional mode. *ECP* is Enhanced Capabilities Port mode, a high-speed bi-directional mode.
Base I/O address	• **378 (default)** • 278	Specifies the base I/O address for the parallel port.
Interrupt	• IRQ 5 • **IRQ 7 (default)**	Specifies the interrupt for the parallel port.
Audio Device	• Disabled • **Enabled (default)**	Enables or disables the onboard audio subsystem.
LAN Device	• Disabled • **Enabled (default)**	Enables or disables the optional onboard 10/100 Ethernet.
Legacy USB Support	• Disabled • **Enabled (default)**	Enables or disables Legacy USB support.

4.4.4 IDE Configuration Submenu

To access this submenu, select Advanced on the menu bar, then IDE Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Extended Configuration
PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 65 is used to configure IDE device options.

Table 65. IDE Device Configuration

Feature	Options	Description
IDE Controller	• Disabled • Primary • Secondary • **Both (default)**	Specifies the integrated IDE controller. *Primary* enables only the Primary IDE Controller. *Secondary* enables only the Secondary IDE Controller. *Both* enables both IDE controllers.
Hard Disk Pre-Delay	• **Disabled (default)** • 3 Seconds • 6 Seconds • 9 Seconds • 12 Seconds • 15 Seconds • 21 Seconds • 30 Seconds	Specifies the hard disk drive pre-delay.
Primary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Master submenu.
Primary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Slave submenu.
Secondary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Master submenu.
Secondary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Slave submenu.

4.4.4.1 Primary/Secondary IDE Master/Slave Submenus

To access these submenus, select Advanced on the menu bar, then IDE Configuration, and then the master or slave to be configured.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Extended Configuration
PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration **Primary IDE Master** **Primary IDE Slave** **Secondary IDE Master** **Secondary IDE Slave**
Diskette Configuration
Event Log Configuration
Video Configuration

There are four IDE submenus: primary master, primary slave, secondary master, and secondary slave. Table 66 shows the format of the IDE submenus. For brevity, only one example is shown.

Table 66. IDE Configuration Submenus

Feature	Options	Description
Drive Installed	No options	Displays the type of drive installed.
Type	• None • User • **Auto (default)** • CD-ROM • ATAPI Removable • Other ATAPI • IDE Removable	Specifies the IDE configuration mode for IDE devices. *User* allows the user to change the LBA Mode Control, Multi-Sector Transfers, PIO Mode, and Ultra DMA settings. *Auto* automatically sets the LBA Mode Control, Multi-Sector Transfers, PIO Mode, and Ultra DMA settings.
Maximum Capacity	No options	Displays the capacity of the drive.
LBA Mode Control	• Disabled • **Enabled (default)**	Enables or disables the LBA mode control.
Multi-Sector Transfers	• Disabled • 2 Sectors • 4 Sectors • 8 Sectors • **16 Sectors (default)**	Specifies number of sectors per block for transfers from the hard disk drive to memory. Check the hard disk drive's specifications for optimum setting.
PIO Mode	• **Auto (default)** • 0 • 1 • 2 • 3 • 4	Specifies the method for moving data to/from the drive.

continued

Table 67. IDE Configuration Submenus (continued)

Feature	Options	Description
Ultra DMA	• **Disabled (default)** • Mode 0 • Mode 1 • Mode 2 • Mode 3 • Mode 4	Specifies the Ultra DMA mode for the drive.
Cable Detected	No options	Displays the type of cable connected to the IDE interface: 40-conductor or 80-conductor (for ATA-100 peripherals).

4.4.5 Diskette Configuration Submenu

To access this menu, select Advanced on the menu bar, then Diskette Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Extended Configuration
PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 67 is used to configure the diskette drive.

Table 67. Diskette Configuration Submenu

Feature	Options	Description
Diskette Controller	• Disabled • **Enabled (default)**	Disables or enables the integrated diskette controller.
Floppy A:	• Not Installed • 360 KB, 5¼″ • 1.2 MB, 5¼″ • 720 KB, 3½″ • **1.44/1.25 MB, 3½″ (default)** • 2.88 MB, 3½″	Specifies the capacity and physical size of diskette drive A.
Diskette Write Protect	• **Disabled (default)** • Enabled	Disables or enables write protect for the diskette drive.

4.4.6 Event Log Configuration

To access this menu, select Advanced on the menu bar, then Event Log Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Extended Configuration
PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 68 is used to configure the event logging features.

Table 68. Event Log Configuration Submenu

Feature	Options	Description
Event Log	No options	Indicates if there is space available in the event log.
Event Log Validity	No options	Indicates if the contents of the event log are valid.
View Event Log	No options	Displays the event log.
Clear All Event Logs	• **No (default)** • Yes	Clears the event log after rebooting.
Event Logging	• Disabled • **Enabled (default)**	Enables logging of events.
Mark Events As Read	• **Yes (default)** • No	Marks all events as read.

4.4.7 Video Configuration Submenu

To access this menu, select Advanced on the menu bar, then Video Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Extended Configuration
PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 69 is used to configure video features.

Table 69. Video Configuration Submenu

Feature	Options	Description
Primary Video Adapter	• **AGP (default)** • PCI	Allows the user to select between the onboard direct AGP graphics or the PCI add-in graphics card as primary graphics adapter in a multi-monitor system.

4.5 Security Menu

To access this menu, select Security from the menu bar at the top of the screen.

Maintenance	Main	Advanced	**Security**	Power	Boot	Exit

The menu represented in Table 70 is used to set passwords and security features.

Table 70. Security Menu

Feature	Options	Description
Supervisor Password Is	No options	Reports if there is a supervisor password set.
User Password Is	No options	Reports if there is a user password set.
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
Clear User Password (Note 1)	No options	Clears the user password.
User Access Level (Note 2)	• Limited • No Access • View Only • **Full (default)**	Specifies the amount of user access to the Setup program. *Limited* allows only limited fields to be changed. *No Access* prevents user access. *View Only* allows the user to view but not change the fields in the Setup program. *Full* allows any field to be changed except the supervisor password.
Unattended Start (Note 1)	• **Disabled (default)** • Enabled	Enabled allows system to complete the boot process without a password. The keyboard remains locked until a password is entered. A password is required to boot from a diskette.

Notes:

1. This feature appears only if a user password has been set.
2. This feature appears only if a supervisor password has been set.

4.6 Power Menu

To access this menu, select Power from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit

The menu represented in Table 71 is used to set the power management features.

Table 71. Power Menu

Feature	Options	Description
Power Management	• Disabled • **Enabled (default)**	Enables or disables the APM BIOS power management feature. (Note)
Inactivity Timer	• Off • 1 Minute • 5 Minutes • 10 Minutes • **20 Minutes (default)** • 30 Minutes • 60 Minutes • 120 Minutes	Specifies the amount of time before the computer enters standby mode, when APM power management is active. (Note)
Hard Drive	• Disabled • **Enabled (default)**	Enables or disables power management for hard disks during standby and suspend modes, when APM power management is active. (Note)
ACPI Suspend State	• **S1 State (default**) • S3 State	Selects the suspend state the system will use when ACPI power management is active. To enable an instantly available configuration, this must be set to the S3 state and an operating system which fully supports the ACPI S3 suspend state must be installed.
Video Repost	• **Disabled (default)** • Enabled	Allows video BIOS to be initialized coming out of S3. This option is present only when ACPI Suspend State is set to S3.

Note: Power Management, Inactivity Timer, and Hard Drive features apply only for APM operating systems.

4.7 Boot Menu

To access this menu, select Boot from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit

The menu represented in Table 72 is used to set the boot features and the boot sequence.

Table 72. Boot Menu

Feature	Options	Description
Quiet Boot	• Disabled • **Enabled (default)**	*Disabled* displays normal POST messages. *Enabled* displays the OEM logo instead of POST messages.
Intel Rapid BIOS Boot	• Disabled • **Enabled (default)**	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	• **Disabled (default)** • Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
After Power Failure	• Stays Off • **Last State (default)** • Power On	Specifies the mode of operation if an AC/Power loss occurs. *Power On* restores power to the computer. *Stay Off* keeps the power off until the power button is pressed. *Last State* restores the previous power state before power loss occurred.
On Modem Ring	• **Stay Off (default)** • Power On	Specifies how the computer responds to an incoming call on an installed modem when the power is off.
On LAN	• **Stay Off (default)** • Power On	Specifies how the computer responds to a LAN wakeup event when the power is off.
On PME	• **Stay Off (default)** • Power On	Specifies how the computer responds to a PME wakeup event when the power is off.
1st Boot Device 2nd Boot Device 3rd Boot Device 4th Boot Device 5th Boot Device	• Floppy • ARMD-FDD (Note 1) • ARMD-HDD (Note 2) • IDE-HDD • ATAPI CD-ROM • Intel UNDI, PXE 2.0 (build 071) (Note 3) • Disabled	Specifies the boot sequence from the available devices. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device. The operating system assigns a drive letter to each boot device in the order listed. Changing the order of the devices changes the drive lettering. The default settings for the first through fifth boot devices are, respectively: • Floppy • IDE-HDD • ATAPI CD-ROM • Intel UNDI • Disabled

continued

Table 72. Boot Menu (continued)

Feature	Options	Description
IDE Drive Configuration	No Options	Configures IDE drives. When selected, displays the IDE Drive Configuration submenu.

Notes:

1. ARMD-FDD = ATAPI removable device - floppy disk drive
2. ARMD-HDD = ATAPI removable device - hard disk drive
3. UNDI = Universal Network Interface Card (NIC) Driver Interface
   PXE = Pre-boot eXecution Environment

4.8 Exit Menu

To access this menu, select Exit from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	Boot	**Exit**

The menu represented in Table 73 is used to exit the Setup program, saving changes, and loading and saving defaults.

Table 73. Exit Menu

Feature	Description
Exit Saving Changes	Exits and saves the changes in CMOS SRAM.
Exit Discarding Changes	Exits without saving any changes made in the Setup program.
Load Setup Defaults	Loads the factory default values for all the Setup options.
Load Custom Defaults	Loads the custom defaults for Setup options.
Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
Discard Changes	Discards changes without exiting the Setup program. The option values present when the computer was turned on are used.

5 Error Messages and Beep Codes

What This Chapter Contains

5.1 BIOS Error Messages

Table 74 lists the error messages and provides a brief description of each.

Table 74. BIOS Error Messages

Error Message	Explanation
GA20 Error	An error occurred with Gate-A20 when switching to protected mode during the memory test.
Pri Master HDD Error Pri Slave HDD Error Sec Master HDD Error Sec Slave HDD Error	Could not read sector from corresponding drive.
Pri Master Drive – ATAPI Incompatible Pri Slave Drive – ATAPI Incompatible Sec Master Drive – ATAPI Incompatible Sec Slave Drive – ATAPI Incompatible	Corresponding drive is not an ATAPI device. Run Setup to make sure device is selected correctly.
A: Drive Error	No response from diskette drive.
Cache Memory Error	An error occurred while testing L2 cache. Cache memory may be bad.
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Display Type Wrong	The display type is different than what has been stored in CMOS. Check Setup to make sure type is correct.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
CMOS Settings Wrong	CMOS values are not the same as the last boot. These values have either been corrupted or the battery has failed.
CMOS Date/Time Not Set	The time and/or date values stored in CMOS are invalid. Run Setup to set correct values.
DMA Error	Error during read/write test of DMA controller.
FDC Failure	Error while trying to access diskette drive controller.
HDC Failure	Error while trying to access hard disk controller.
Update Failed	NVRAM was invalid but was unable to be updated.

continued

Table 74. BIOS Error Messages (continued)

Error Message	Explanation
Unlock Keyboard	The system keyboard lock is engaged. The system must be unlocked to continue to boot.
Keyboard Error	Error in the keyboard connection. Make sure keyboard is connected properly.
KB/Interface Error	Keyboard Interface Test failed.
Timer Error	Timer Test failed.
Memory Size Changed	Memory size has changed since the last boot. If no memory was added or removed, then memory may be bad.
Serial presence detect (SPD) device data missing or inconclusive. Do you wish to boot at 100 MHz bus speed? [Y/N]	System memory does not appear to be SPD memory.
No Boot Device Available	System did not find a boot device.
Off Board Parity Error	A parity error occurred on an offboard card. This error is followed by an address.
On Board Parity Error	A parity error occurred in onboard memory. This error is followed by an address.
Parity Error	A parity error occurred in onboard memory at an unknown address.
NVRAM / CMOS / PASSWORD cleared by Jumper	NVRAM, CMOS, and passwords have been cleared. The system should be powered down and the jumper removed.
<CTRL_N> Pressed	CMOS is ignored and NVRAM is cleared. User must enter Setup.

5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires an add-in card (often called a POST card). The POST card can decode the port and display the contents on a medium such as a seven-segment display. These cards can be purchased from JDR Microdevices or other sources.

The tables below offer descriptions of the POST codes generated by the BIOS. Table 75 defines the Uncompressed INIT Code Checkpoints,

Table 76 describes the Boot Block Recovery Code Checkpoints, and Table 77 lists the Runtime Code Uncompressed in F000 Shadow RAM. Some codes are repeated in the tables because that code applies to more than one operation.

Table 75. Uncompressed INIT Code Checkpoints

Code	Description of POST Operation
D0	NMI is disabled. Onboard keyboard controller and real time clock enabled (if present). Initialization code checksum verification starting.
D1	Keyboard controller BAT test, CPU ID saved, and going to 4 GB flat mode.
D3	Initialize chipset, start memory refresh, and determine memory size.
D4	Verify base memory.
D5	Initialization code to be copied to segment 0 and control to be transferred to segment 0.
D6	Control is in segment 0. Used to check if in recovery mode and to verify main BIOS checksum. If in recovery mode or if main BIOS checksum is wrong, go to check point E0 for recovery. Otherwise, go to check point D7 to give control to main BIOS.
D7	Find main BIOS module in ROM image.
D8	Uncompress the main BIOS module.
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM.

Table 76. Boot Block Recovery Code Checkpoints

Code	Description of POST Operation
E0	Onboard diskette controller (if any) is initialized. Compressed recovery code is uncompressed at F000:0000 in shadow RAM. Give control to recovery code at F000 in shadow RAM. Initialize interrupt vector tables, system timer, DMA controller, and interrupt controller.
E8	Initialize extra (Intel recovery) module.
E9	Initialize diskette drive.
EA	Try to boot from diskette. If reading of boot sector is successful, give control to boot sector code.
EB	Boot from diskette failed; look for ATAPI (LS-120, Zip) devices.
EC	Try to boot from ATAPI device. If reading of boot sector is successful, give control to boot sector code.
EF	Boot from diskette and ATAPI device failed. Give two beeps. Retry the booting procedure (go to check point E9).

Table 77. Runtime Code Uncompressed in F000 Shadow RAM

Code	Description of POST Operation
03	NMI is Disabled. Check soft reset/power-on.
05	BIOS stack set. Disable cache if any.
06	Uncompress POST code.
07	Initialize processor and initialize processor data area.
08	Next, calculate CMOS checksum.
0B	Next, do any initialization before executing keyboard BAT.
0C	Keyboard controller I/B free. Issue the BAT command to keyboard controller.
0E	Any initialization after keyboard controller BAT to be done next.
0F	Write keyboard command byte.
10	Issue pin 23, 24 blocking/unblocking command.
11	Check whether <INS>, <END> keys were pressed during power on.
12	Initialize CMOS if "Init CMOS in every boot" is set or if <END> key is pressed. Then disable DMA and interrupt controllers.
13	Video display is disabled and port B is initialized. Chipset initialization about to begin.
14	8254 Timer Test is about to start.
19	Memory Refresh Test is about to start.
1A	Memory Refresh line is toggling. Check 15 µs ON/OFF time.
23	Read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable.
24	Do any setup before interrupt vector initialization.
25	Interrupt vector initialization to begin. Clear password if necessary.
27	Next, do any initialization before setting video mode.
28	Set monochrome mode and color mode.
2A	Start initialization of different buses, if present (system, static, output devices). (See Section 5.3 for details of different buses.)
2B	Give control for any setup required before optional video ROM check.
2C	Look for optional video ROM and give control.
2D	Give control to do any processing after video ROM returns control.
2E	If EGA/VGA not found, then execute Display Memory R/W Test.
2F	EGA/VGA not found. Display Memory R/W Test about to begin.
30	Display Memory R/W Test passed. Look for the retrace checking.
31	Display Memory R/W Test or retrace checking failed. Do Alternate Display Memory R/W Test.
32	Alternate Display Memory R/W Test passed. Look for the alternate display retrace checking.
34	Video display checking complete. Next, set display mode.
37	Display mode set. Then display the power-on message.
38	Start initialization of different buses, if present (input, IPL, general devices). (See Section 5.3 for details of different buses.)
39	Display different buses initialization error messages. (See Section 5.3 for details of different buses.)
3A	New cursor position read and saved. Ready to display the Hit <DEL> message.

continued

Table 77. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
40	Prepare the descriptor tables.
42	Enter virtual mode for memory test.
43	Enable interrupts for diagnostics mode.
44	Initialize data to check memory wrap-around at 0:0.
45	Data initialized. Check for memory wrap-around at 0:0, and find the total system memory size.
46	Memory wrap-around test done. Memory size calculation complete. Ready to write patterns to test memory.
47	Pattern to be tested written in extended memory. Next, write patterns in base 640 K memory.
48	Patterns written in base memory. Find amount of memory below 1 MB.
49	Amount of memory below 1 MB found and verified. Find out amount of memory above 1 MB.
4B	Amount of memory above 1 MB found and verified. Check for soft reset and clear memory below 1 MB for soft reset. (If power on, go to check point 4Eh).
4C	Memory below 1 MB cleared. (Soft reset) Clear memory above 1 MB.
4D	Memory above 1 MB cleared. (Soft reset) Save the memory size. (Go to checkpoint 52h).
4E	Memory test started. (Not Soft Reset) Ready to display the first 64 K memory size.
4F	Memory size display started. This will be updated during memory test. Run sequential and random memory test.
50	Memory testing/initialization below 1MB complete. Ready to adjust displayed memory size for relocation/shadow.
51	Memory size display adjusted due to relocation/shadow. Memory test above 1 MB to follow.
52	Memory testing/initialization above 1 MB complete. Ready to save memory size information.
53	Memory size information is saved. Processor registers are saved. Ready to enter real mode.
54	Shutdown successful, processor in real mode. Ready to disable gate A20 line and disable parity/NMI.
57	Successfully disabled A20 address line and parity/NMI. Ready to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Ready to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. Ready to start DMA and Interrupt Controller Test.
60	DMA Page Register Test passed. Ready to start DMA#1 Base Register Test.
62	DMA#1 Base Register Test passed. Ready to start DMA#2 Base Register Test.
65	DMA#2 Base Register Test passed. Ready to program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming complete. Ready to initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck key. Next, issue keyboard reset command.
81	Keyboard reset error/stuck key found. Ready to issue keyboard controller interface test command.
82	Keyboard controller interface test complete. Ready to write command byte and initialize circular buffer.
83	Command byte written, global data initialization complete. Check for lock-key.

continued

Table 77. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
84	Lock-key checking complete. Next, check for memory size mismatch with CMOS.
85	Memory size check complete. Next, display soft error and check for password or bypass Setup.
86	Password checked. Ready to do programming before Setup.
87	Programming before Setup complete. Uncompress Setup code and execute.
88	Returned from CMOS Setup program and cleared screen. Ready to do programming after Setup.
89	Programming after Setup complete. Display power-on message.
8B	First screen message displayed. <WAIT...> message displayed. PS/2 mouse check and extended BIOS data area allocation to be done.
8C	Ready to start Setup options programming.
8D	Ready to reset hard disk controller.
8F	Hard disk controller reset complete. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
95	Start initialization of different buses optional ROMs from C800. (See Section 5.3 for details of different buses.)
96	Ready to do any init before C800 optional ROM control.
97	Any initialization before C800 optional ROM control is complete. Next, do optional ROM check and control.
98	Optional ROM control is complete. Next, give control to do any required processing after optional ROM returns control and enable external cache.
99	Do any initialization required after optional ROM Test is over. Ready to set up timer data area and printer base address.
9A	Return after setting timer and printer base address. Ready to set the RS-232 base address.
9B	Returned after RS-232 base address. Ready to do any initialization before coprocessor test.
9C	Required initialization before coprocessor test is complete. Ready to initialize coprocessor next.
9D	Coprocessor initialized. Ready to do any initialization after Coprocessor Test.
9E	Initialization after Coprocessor Test is complete. Ready to check extended keyboard, keyboard ID, and NumLock.
A2	Ready to display any soft errors.
A3	Soft error display complete. Ready to set keyboard typematic rate.
A4	Keyboard typematic rate set. Ready to program memory wait states.
A5	Ready to enable parity/NMI.
A7	NMI and parity enabled. Ready to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control complete. E000 ROM to get control next.
A9	Returned from E000 ROM control. Ready to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control complete. Ready to display the system configuration.
AB	Put INT13 module runtime image to shadow RAM.
AC	Generate MP for multiprocessor support, if present.

continued

Table 77. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
AD	Put CGA INT10 module, if present, in shadow RAM.
AE	Uncompress SMBIOS module, initialize SMBIOS code, and form the runtime SMBIOS image in shadow RAM.
B1	Ready to copy any code to specific area.
00	Copying of code to specific area complete. Ready to give control to INT19 boot loader.

5.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at the following checkpoints to do various tasks. Table 78 describes the bus initialization checkpoints.

Table 78. Bus Initialization Checkpoints

Checkpoint	Description
2A	Different buses init (system, static, output devices) to start, if present.
38	Different buses init (input, IPL, general devices) to start, if present.
39	Display different buses initialization error messages.
95	Initialization of different buses optional ROMs from C800 to start.

While control is inside the different bus routines, additional checkpoints are output to port 80h as word values to identify the routines under execution. In these word-value checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. Table 79 describes the upper nibble of the high byte and indicates the function being executed.

Table 79. Upper Nibble High Byte Functions

Value	Description
0	func#0, disable all devices on this bus
1	func#1, initialize static devices on this bus
2	func#2, initialize output device on this bus
3	func#3, initialize input device on this bus
4	func#4, initialize IPL device on this bus
5	func#5, initialize general device on this bus
6	func#6, report errors on this bus
7	func#7, initialize add-on ROM on all buses

Table 80 describes the lower nibble of the high byte and indicates the bus on which the routines are being executed.

Table 80. Lower Nibble High Byte Functions

Value	Description
0	Generic DIM (Device Initialization Manager)
1	Onboard system devices
2	ISA devices
3	EISA devices
4	ISA PnP devices
5	PCI devices

5.4 Speaker

A 47 Ω inductive speaker is mounted on the board. The speaker provides audible error code (beep code) information during the power-on self-test (POST).

For information about	Refer to
The location of the onboard speaker	Figure 1, page 14

5.5 BIOS Beep Codes

Whenever a recoverable error occurs during power-on self-test (POST), the BIOS displays an error message describing the problem (see Table 81). The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video card or no card installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 81. Beep Codes

Beep	Description
1	Refresh failure
2	Parity cannot be reset
3	First 64 KB memory failure
4	Timer not operational
5	Not used
6	8042 GateA20 cannot be toggled
7	Exception interrupt error
8	Display memory R/W error
9	Not used
10	CMOS Shutdown register test error
11	Invalid BIOS (e.g. POST module not found, etc.)