VS440FX Motherboard Specification Update

Release Date: July 1997

Order Number: 281813-012

The VS440FX motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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P.O. Box 7641
Mt. Prospect, IL 60056-7641

or call in North America 1-800-879-4683, Europe 44-0-1793-431-155, France 44-0-1793-421-777,

Germany 44-0-1793-421-333, other Countries 708-296-9333

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REVISION HISTORY

Date of Revision	Version	Description
June 1996	-001	This document is the first Specification Update for the Intel VS440FX motherboard.
July 1996	-002	Added Erratum 3.
August 1996	-003	Updated General Information.
September 1996	-004	Added Erratum 4 and Documentation Changes 1-4.
November 1996	-005	Added Errata 5-6. Removed Documentation Changes 1-4, which were incorporated into revision -003 of the specification.
December 1996	-006	Added Erratum 7 and Specification Clarification 1.
January 1997	-007	Added Errata 8-9. Updated status of Errata 3 and 7.
March 1997	-008	Added Documentation Change 1.
April 1997	-009	Added Errata 10-11. Added Documentation Changes 2-3. Updated status of Erratum 9. Revised format of PBA/BIOS revision table.
May 1997	-010	Modified Erratum 8.
June 1997	-011	Added Specification Clarifications 2-4 and Documentation Change 4.
July 1997	-012	Added Erratum 12, Specification Clarification 5 and Documentation Changes 5-6.

PREFACE

This document is an update to the specifications contained in the *VS440FX Motherboard Technical Product Specification* (Order Number 281812). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Pentium® Pro Processor Specification Update* (Order Number 242689) for specification updates concerning the Pentium® Pro processor. Items contained in the *Pentium® Pro Processor Specification Update* that either do not apply to the VS440FX motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the PBA revision(s) associated with that stepping.

Refer to the *82440FX PCIset Specification Update* (Order Number 297654) for specification updates concerning the 82440FX PCIset. Items contained in the *82440FX PCIset Specification Update* that either do not apply to the VS440FX motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any PCIset errata for a given stepping are applicable to the PBA revision(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the VS440FX motherboard's behavior to deviate from published specifications. Hardware and software designed to be used with any given Printed Board Assembly (PBA) and BIOS revision level must assume that all errata documented for that PBA and BIOS revision level are present on all motherboards.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Update for VS440FX Motherboards

GENERAL INFORMATION

Basic VS440FX Motherboard Identification Information

AA Revision	PBA Revision	82440FX PCISet Stepping	BIOS Revision	Notes
655391-404	655390-404	A1	1.00.03.CS1	1, 2, 4, 5, 6
655391-405	655390-405	A1	1.00.04.CS1	1, 2, 4, 5, 6
655391-406	655390-406	A1	1.00.05.CS1	1, 3, 4, 5, 7
655391-407	655390-407	A1	1.00.05.CS1	1, 3, 4, 5, 7
655391-408	655390-408	A1	1.00.06.CS1	1, 3, 4, 5, 7
655391-428	655390-428	A1	1.00.06.CS1	1, 3, 4, 5, 7
655391-503	655390-503	A1	1.00.09.CS1	1, 3, 4, 5, 7
655391-504	655390-504	A1	1.00.11.CS1	1, 3, 4, 5, 7
655391-505	655390-505	A1	1.00.11.CS1	1, 3, 4, 5, 7
659299-404	655390-404	A1	1.00.03.CS1	1, 2, 4, 5, 6
659299-405	655390-405	A1	1.00.04.CS1	1, 2, 4, 5, 6
659299-406	655390-406	A1	1.00.05.CS1	1, 3, 4, 5, 7
659299-407	655390-407	A1	1.00.05.CS1	1, 3, 4, 5, 7
659299-408	655390-408	A1	1.00.06.CS1	1, 3, 4, 5, 7
659299-428	655390-428	A1	1.00.06.CS1	1, 3, 4, 5, 7
659299-503	655390-503	A1	1.00.09.CS1	1, 3, 4, 5, 7
659299-504	655390-504	A1	1.00.11.CS1	1, 3, 4, 5, 7
655391-505	655390-505	A1	1.00.11.CS1	1, 3, 4, 5, 7
663973-506	661105-506	A1	1.00.09.CS1	1, 3, 4, 5, 7
663973-507	661105-507	A1	1.00.11.CS1	1, 3, 4, 5, 7
663973-508	661105-508	A1	1.00.11.CS1	1, 3, 4, 5, 7
663941-505	663900-505	A1	1.00.09.CS1	1, 3, 4, 5, 7
663941-506	663900-506	A1	1.00.11.CS1	1, 3, 4, 5, 7
663941-507	663900-507	A1	1.00.11.CS1	1, 3, 4, 5, 7
665558-410	665559-410	A1	1.00.09.CS1	1, 3, 4, 5, 7
665558-502	665559-502	A1	1.00.11.CS1	1, 3, 4, 5, 7
660849-408	660822-408	A1	1.00.05.CS1	1, 3, 4, 5, 7
660849-409	660822-409	A1	1.00.05.CS1	1, 3, 4, 5, 7
660849-410	660822-410	A1	1.00.06.CS1	1, 3, 4, 5, 7
660849-411	660822-411	A1	1.00.09.CS1	1, 3, 4, 5, 7
660849-412	660822-412	A1	1.00.11.CS1	1, 3, 4, 5, 7

NOTES:

1. The PBA number is found on a small label on the component side of the board.
2. The 82440FX PCIset kit used on this PBA revision consists of three components as follows:

Device	Stepping	S-Spec Numbers
82441FX	A1	SU053
82442FX	A1	SU054
82371SB	A1	SU052

3. The 82440FX PCIset kit used on this PBA revision consists of three components as follows:

Device	Stepping	S-Spec Numbers
82441FX	A1	SU053
82442FX	A1	SU054
82371SB	B0	SU093

4. The following errata are contained in the *Pentium® Pro Processor Specification Update* (Order Number 242689) for the Pentium® Pro processor and either do not apply to the VS440FX motherboard or have been worked-around in this PBA and/or BIOS revision: 1, 4, 14-15, 25, 41, 50 and 1AP-8AP. All other errata associated with the processor apply to this PBA revision.
5. The following items are contained in the *Intel 440FX PCIset Specification Update* (Order Number 297654) and either do not apply to the VS440FX motherboard or have been worked around in this PBA and/or BIOS revision:
   82441FX (PMC) Erratum 2.
   All other errata associated with the PCIset apply to this PBA revision.
6. The following errata contained in the *82371SB PIIX3 Specification Update* (Order Number 297658) either do not apply to the VS440FX motherboard or have been worked around in this PBA and/or BIOS revision: 1-3, 13. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82371SB PIIX3 Specification Update*.
7. The following items are contained in the *82371SB PIIX3 Stepping Information* (Order Number 297658) and either do not apply to the VS440FX motherboard or have been worked around in this PBA and/or BIOS revision: 1-9, 13.
   All other errata associated with the PIIX3 apply to this PBA revision.

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the VS440FX motherboard. Intel intends to fix some of the errata in a future revision of the motherboard, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future revision of the motherboard or BIOS.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	PLANS	SPECIFICATION CHANGES
1	Doc	Only Processors With 256 Kbytes of Cache Are Supported
NO.	**PLANS**	**ERRATA**
1	NoFix	CS32DIAG conflicts with CrystalWare* Audio CD Player
2	Fixed	PCI Delayed Transactions are not supported
3	Fixed	External chassis speaker is not supported
4	Fix	Audio track of CD-ROM game does not play in Microsoft Windows* 95
5	Fix	BIOS does not support no-emulation mode for CD-ROM boot
6	Fix	System may prevent configuration of ISA Plug and Play add-in cards
7	Fixed	CMOS checksum may be lost if power is cycled during boot
8	NoFix	Video capture card may hang system due to improper TRST# signal
9	Fixed	System may hang at boot due to incorrect 60 ns memory timings
10	NoFix	Cannot meet FCC Class B requirements using unshielded USB cable
11	Fix	System BIOS does not recognize bootable USB devices
12	Fix	Management extension ASIC may fail to reset at power-on
NO.	**PLANS**	**SPECIFICATION CLARIFICATIONS**
1	Doc	Enabling Interrupts in System Management Mode (SMM)
2	Doc	Advanced Power Management (APM) will not function as expected with Universal Serial Bus (USB) enabled
3	Doc	64 MB SIMM*s will cause performance degradation
4	Doc	PCI 2.1 Specification optional features
5	Doc	Administrator and user passwords

NO.	PLANS	DOCUMENTATION CHANGES
1	Doc	Change description of auxiliary fan connector for some motherboards
2	Doc	Revise IO address for management extension hardware
3	Doc	Add support for 3.5 V processors
4	Doc	Revision of Section 5.1, *Specifications*
5	Doc	Revision of Section 1.7.1, *82441FX PCI Bridge and Memory Controller (PMC)*
6	Doc	Change to description of serial port capabilities

The errata described in the specification update apply to combinations of PBA revision and BIOS revision as shown in this table:

PBA Revision	BIOS Revision	Errata That Apply to This Combination
655390-404	1.00.02.CS1‡	3, 5-9
	1.00.03.CS1‡	3, 5-9
	1.00.04.CS1	3, 5-9
	1.00.05.CS1	3, 5-9
	1.00.06.CS1	3, 5-9
	1.00.07.CS1	3, 5-9
	1.00.08.CS1	3, 5-6, 8-9
	1.00.09.CS1	3, 5-6, 8-9
	1.00.11.CS1	3, 5-6, 8
655390-405	1.00.02.CS1‡	3, 5-9
	1.00.03.CS1‡	3, 5-9
	1.00.04.CS1	3, 5-9
	1.00.05.CS1	3, 5-9
	1.00.06.CS1	3, 5-9
	1.00.07.CS1	3, 5-9
	1.00.08.CS1	3, 5-6, 8-9
	1.00.09.CS1	3, 5-6, 8-9
	1.00.11.CS1	3, 5-6, 8
655390-406	1.00.02.CS1‡	3, 5-9
	1.00.03.CS1‡	3, 5-9
	1.00.04.CS1‡	3, 5-9
	1.00.05.CS1	3, 5-9
	1.00.06.CS1	3, 5-9
	1.00.07.CS1	3, 5-9
	1.00.08.CS1	3, 5-6, 8-9
	1.00.09.CS1	3, 5-6, 8-9
	1.00.11.CS1	3, 5-6, 8

PBA Revision	BIOS Revision	Errata That Apply to This Combination
655390-407	1.00.02.CS1‡	3, 5-9
	1.00.03.CS1‡	3, 5-9
	1.00.04.CS1‡	3, 5-9
	1.00.05.CS1	3, 5-9
	1.00.06.CS1	3, 5-9
	1.00.07.CS1	3, 5-9
	1.00.08.CS1	3, 5-6, 8-9
	1.00.09.CS1	3, 5-6, 8-9
	1.00.11.CS1	3, 5-6, 8
655390-408	1.00.02.CS1‡	3, 5-9
	1.00.03.CS1‡	3, 5-9
	1.00.04.CS1‡	3, 5-9
	1.00.05.CS1‡	3, 5-9
	1.00.06.CS1	3, 5-9
	1.00.07.CS1	3, 5-9
	1.00.08.CS1	3, 5-6, 8-9
	1.00.09.CS1	3, 5-6, 8-9
	1.00.11.CS1	3, 5-6, 8
655390-428	1.00.02.CS1‡	3, 5-9
	1.00.03.CS1‡	3, 5-9
	1.00.04.CS1‡	3, 5-9
	1.00.05.CS1‡	3, 5-9
	1.00.06.CS1	3, 5-9
	1.00.07.CS1	3, 5-9
	1.00.08.CS1	3, 5-6, 8-9
	1.00.09.CS1	3, 5-6, 8-9
	1.00.11.CS1	3, 5-6, 8

PBA Revision	BIOS Revision	Errata That Apply to This Combination
655390-503	1.00.02.CS1‡	5-9
	1.00.03.CS1‡	5-9
	1.00.04.CS1‡	5-9
	1.00.05.CS1‡	5-9
	1.00.06.CS1‡	5-9
	1.00.07.CS1‡	5-9
	1.00.08.CS1‡	5-6, 8-9
	1.00.09.CS1	5-6, 8-9
	1.00.11.CS1	5-6, 8
655390-504	1.00.02.CS1‡	5-9
	1.00.03.CS1‡	5-9
	1.00.04.CS1‡	5-9
	1.00.05.CS1‡	5-9
	1.00.06.CS1‡	5-9
	1.00.07.CS1‡	5-9
	1.00.08.CS1‡	5-6, 8-9
	1.00.09.CS1‡	5-6, 8-9
	1.00.11.CS1	5-6, 8
655390-505	1.00.02.CS1‡	5-9
	1.00.03.CS1‡	5-9
	1.00.04.CS1‡	5-9
	1.00.05.CS1‡	5-9
	1.00.06.CS1‡	5-9
	1.00.07.CS1‡	5-9
	1.00.08.CS1‡	5-6, 8-9
	1.00.09.CS1‡	5-6, 8-9
	1.00.11.CS1	5-6, 8
661105-506	1.00.02.CS1‡	1, 4-12
	1.00.03.CS1‡	1, 4-12
	1.00.04.CS1‡	1, 4-12
	1.00.05.CS1‡	1, 4-12
	1.00.06.CS1‡	1, 4-12
	1.00.07.CS1‡	1, 4-12
	1.00.08.CS1‡	1, 4-6, 8-12
	1.00.09.CS1	1, 4-6, 8-12
	1.00.11.CS1	1, 4-6, 8, 10-12

PBA Revision	BIOS Revision	Errata That Apply to This Combination
661105-507	1.00.02.CS1‡	1, 4-12
	1.00.03.CS1‡	1, 4-12
	1.00.04.CS1‡	1, 4-12
	1.00.05.CS1‡	1, 4-12
	1.00.06.CS1‡	1, 4-12
	1.00.07.CS1‡	1, 4-12
	1.00.08.CS1‡	1, 4-6, 8-12
	1.00.09.CS1‡	1, 4-6, 8-12
	1.00.11.CS1	1, 4-6, 8, 10-12
661105-508	1.00.02.CS1‡	1, 4-12
	1.00.03.CS1‡	1, 4-12
	1.00.04.CS1‡	1, 4-12
	1.00.05.CS1‡	1, 4-12
	1.00.06.CS1‡	1, 4-12
	1.00.07.CS1‡	1, 4-12
	1.00.08.CS1‡	1, 4-6, 8-12
	1.00.09.CS1‡	1, 4-6, 8-12
	1.00.11.CS1	1, 4-6, 8, 10-12
663900-505	1.00.02.CS1‡	5-12
	1.00.03.CS1‡	5-12
	1.00.04.CS1‡	5-12
	1.00.05.CS1‡	5-12
	1.00.06.CS1‡	5-12
	1.00.07.CS1‡	5-12
	1.00.08.CS1‡	5-6, 8-12
	1.00.09.CS1	5-6, 8-12
	1.00.11.CS1	5-6, 8, 10-12

PBA Revision	BIOS Revision	Errata That Apply to This Combination
663900-506	1.00.02.CS1‡	5-12
	1.00.03.CS1‡	5-12
	1.00.04.CS1‡	5-12
	1.00.05.CS1‡	5-12
	1.00.06.CS1‡	5-12
	1.00.07.CS1‡	5-12
	1.00.08.CS1‡	5-6, 8-12
	1.00.09.CS1‡	5-6, 8-12
	1.00.11.CS1	5-6, 8, 10-12
663900-507	1.00.02.CS1‡	5-12
	1.00.03.CS1‡	5-12
	1.00.04.CS1‡	5-12
	1.00.05.CS1‡	5-12
	1.00.06.CS1‡	5-12
	1.00.07.CS1‡	5-12
	1.00.08.CS1‡	5-6, 8-12
	1.00.09.CS1‡	5-6, 8-12
	1.00.11.CS1	5-6, 8, 10-12
665559-410	1.00.02.CS1‡	1, 3-9
	1.00.03.CS1‡	1, 3-9
	1.00.04.CS1‡	1, 3-9
	1.00.05.CS1‡	1, 3-9
	1.00.06.CS1‡	1, 3-9
	1.00.07.CS1‡	1, 3-9
	1.00.08.CS1‡	1, 3-6, 8-9
	1.00.09.CS1‡	1, 3-6, 8-9
	1.00.11.CS1	1, 3-6, 8

PBA Revision	BIOS Revision	Errata That Apply to This Combination
665559-502	1.00.02.CS1	1, 4-9
	1.00.03.CS1	1, 4-9
	1.00.04.CS1	1, 4-9
	1.00.05.CS1	1, 4-9
	1.00.06.CS1	1, 4-9
	1.00.07.CS1	1, 4-9
	1.00.08.CS1	1, 4-6, 8-9
	1.00.09.CS1	1, 4-6, 8-9
	1.00.11.CS1	1, 4-6, 8
660822-408	1.00.02.CS1‡	1, 3-9
	1.00.03.CS1‡	1, 3-9
	1.00.04.CS1‡	1, 3-9
	1.00.05.CS1	1, 3-9
	1.00.06.CS1	1, 3-9
	1.00.07.CS1	1, 3-9
	1.00.08.CS1	1, 3-6, 8-9
	1.00.09.CS1	1, 3-6, 8-9
	1.00.11.CS1	1, 3-6, 8
660822-409	1.00.02.CS1‡	1, 3-9
	1.00.03.CS1‡	1, 3-9
	1.00.04.CS1‡	1, 3-9
	1.00.05.CS1	1, 3-9
	1.00.06.CS1	1, 3-9
	1.00.07.CS1	1, 3-9
	1.00.08.CS1	1, 3-6, 8-9
	1.00.09.CS1	1, 3-6, 8-9
	1.00.11.CS1	1, 3-6, 8

PBA Revision	BIOS Revision	Errata That Apply to This Combination
660822-410	1.00.02.CS1‡	1, 3-9
	1.00.03.CS1‡	1, 3-9
	1.00.04.CS1‡	1, 3-9
	1.00.05.CS1‡	1, 3-9
	1.00.06.CS1	1, 3-9
	1.00.07.CS1	1, 3-9
	1.00.08.CS1	1, 3-6, 8-9
	1.00.09.CS1	1, 3-6, 8-9
	1.00.11.CS1	1, 3-6, 8
660822-411	1.00.02.CS1‡	1, 3-9
	1.00.03.CS1‡	1, 3-9
	1.00.04.CS1‡	1, 3-9
	1.00.05.CS1‡	1, 3-9
	1.00.06.CS1‡	1, 3-9
	1.00.07.CS1‡	1, 3-9
	1.00.08.CS1‡	1, 3-6, 8-9
	1.00.09.CS1	1, 3-6, 8-9
	1.00.11.CS1	1, 3-6, 8
660822-412	1.00.02.CS1‡	1, 3-9
	1.00.03.CS1‡	1, 3-9
	1.00.04.CS1‡	1, 3-9
	1.00.05.CS1‡	1, 3-9
	1.00.06.CS1‡	1, 3-9
	1.00.07.CS1‡	1, 3-9
	1.00.08.CS1‡	1, 3-6, 8-9
	1.00.09.CS1‡	1, 3-6, 8-9
	1.00.11.CS1	1, 3-6, 8

NOTE:

‡ This combination of BIOS revision and PBA revision has not undergone regression testing. Use of a PBA with down-revision BIOS is an untested combination and is undertaken at the user's risk.

SPECIFICATION CHANGES

The Specification Changes listed in this section apply to the *VS440FX Motherboard Technical Product Specification* (Order Number 281812). All Specification Changes will be incorporated into a future version of that specification.

1. Only Processors With 256 KB of Cache Are Supported

Only Pentium Pro processors with 256 KB of cache have been qualified with the motherboard. References to processors with 512 KB of cache will be removed from Section 1.1, *Overview* and Section 1.5, *Microprocessor*.

ERRATA

1. CS32DIAG Conflicts With CrystalWare* Audio CD Player

PROBLEM: Many DOS audio programs, including the CS4232 audio diagnostic program, set the mixer volume levels for audio CD to zero. The original levels may not be reset when the program is exited.

IMPLICATION: The user will not be able to hear audio CD's after running audio diagnostics until mixer volume levels are reset.

WORKAROUND: Run the Mixer Utility to restore the audio output before playing an audio CD.

STATUS: This erratum will not be fixed.

2. PCI Delayed Transactions Are Not Supported

PROBLEM: An erratum to the A1 stepping of the 82371SB PCI ISA IDE Xcelerator (PIIX3) requires that the option for Delayed Transactions be turned off by the BIOS.

IMPLICATION: System level performance and compatibility are not affected by turning off delayed transactions. The system will be PCI 2.1 compatible and will support all PCI 2.1 compliant cards.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 1.00.02.CS1.

3. External Chassis Speaker is Not Supported

PROBLEM: The signals to the front panel I/O connector (J10H1) that support an external chassis speaker are not connected.

IMPLICATION: An external chassis speaker that uses the standard 1x4-pin connector will not function.

WORKAROUND: None.

STATUS: This erratum was fixed in PBA revisions with revision level -5xx and greater.

4. Audio Track of CD-ROM Game Does Not Play in Microsoft Windows* 95

PROBLEM: The Crystal audio drivers for Microsoft Windows* 95 have audio CD-ROM input muted as the default setting.

IMPLICATION: The user will not hear the audio effects of the game if they are supplied as audio CD-ROM input.

WORKAROUND: Before launching a game that uses audio CD-ROM input for sound effects, open a DOS window to change the default input from Line In to Audio CD-ROM and set the audio CD-ROM volume levels to 75%.

STATUS: This erratum will be fixed in a future revision of the Crystal audio drivers.

5. BIOS Does Not Support No-Emulation Mode for CD-ROM Boot

PROBLEM: The system BIOS does not support booting from an “El Torito” bootable CD-ROM using the no-emulation mode format.

IMPLICATION: Booting from a CD-ROM using no emulation mode is not supported. For example, Microsoft Windows NT* version 4.0 uses no-emulation mode for its boot CD-ROM.

WORKAROUND: Boot the computer from a floppy or hard disk, then install or run the program from the CD-ROM.

STATUS: This erratum will be fixed in a future BIOS revision.

6. System May Prevent Configuration of ISA Plug and Play Add-in Cards

PROBLEM: If the onboard parallel port is configured to use ECP mode at LPT2, an ISA Plug and Play card may not respond to configuration commands.

IMPLICATION: Some ISA Plug and Play cards will not be recognized or properly configured at system boot.

WORKAROUND: Configure the parallel port at LPT1 to use ECP mode or configure LPT2 for a mode other than ECP.

STATUS: This erratum will be fixed in a future PBA revision.

7. CMOS Checksum May Be Lost If Power Is Cycled During Boot

PROBLEM: If the computer power is turned off during a short portion of the boot process, the CMOS checksum byte will not be updated. The next time the computer is turned on, the message “CMOS Checksum Invalid” will be displayed.

IMPLICATION: When the message is displayed, the correct checksum has already been recalculated and stored. No user action is required to recover from the error. If the additional message:

> Date and Time Not Set
> Press <F1> for Setup, <Esc> to Boot

is displayed, the user will have to reset the current date and time using the BIOS Setup program.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 1.00.08.CS1.

8. PCI Add-in Card May Hang System Due to Improper TRST# Signal

PROBLEM: If a PCI add-in card that implements boundary scan is installed, the system may not boot. In accordance with the PCI 2.1 specification, the add-in card expects the TRST# signal to be pulled down if JTAG is not supported by the motherboard. The motherboard does not implement JTAG boundary scan and does not pull the TRST# signal down, which prevents the add-in card from initializing properly.

IMPLICATION: The system may not boot if a PCI card that implements JTAG boundary scan is inserted.

WORKAROUND: None.

STATUS: This erratum will not be fixed.

9. System May Hang at Boot Due to Incorrect 60 ns Memory Timings

PROBLEM: Systems using 60 ns EDO SIMM*s may fail, resulting in no video displayed at initial power-on. The system improperly uses a default value of 38 ns for the Tcsh memory timing parameter at power-on, which may result in a hang condition.

IMPLICATION: Systems may be incompatible with 60 ns EDO SIMMs that cannot function with a Tcsh value of 38 ns.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 1.00.11.CS1.

10. Cannot Meet FCC Class B Requirements Using Unshielded USB Cable

PROBLEM: The motherboard will generate excessive electromagnetic radiation on unshielded USB cables, even if no device or a low speed (sub-channel) USB device is attached to the cable.

IMPLICATION: Systems based on this motherboard will not meet FCC Part 15 Class B requirements when unshielded USB cable is used. Although this condition is a violation of the USB v1.0 specification, it is not believed to have any effect on normal USB device operation.

WORKAROUND: Use USB devices with shielded cable that meet the requirements for high speed (fully-rated) USB devices.

STATUS: This erratum will not be fixed.

11. System BIOS Does Not Recognize Bootable USB Devices

PROBLEM: The system BIOS does not recognize a USB keyboard or mouse during a system boot. A USB keyboard or mouse is not recognized until an operating system that supports USB is loaded.

IMPLICATION: 1. The user is not able to use a USB keyboard to enter the BIOS Setup or to respond to error messages that are displayed before an operating system with USB support is loaded.
2. The user is not able to use a USB keyboard or mouse with any operating system that does not have USB support.

WORKAROUND: Use a standard PS/2* style keyboard and mouse in any configuration where input is required before an operating system with USB support is loaded.

STATUS: This erratum will be fixed in a future BIOS revision.

12. Management Extension ASIC May Fail to Reset at Power-On

PROBLEM: If external system devices, such as monitors or printers, are already powered on at system power-on, they may provide an offset potential of greater than 200 mV DC between the V_{CC} power plane and the ground plane of the motherboard. This can cause an intermittent internal reset failure in the management extension ASIC used on the motherboard. If the internal reset fails, no data conversions will occur and the ASIC registers that store temperature, voltage and fan speed data will be set to zero.

IMPLICATION: If LANDesk® software or other management software attempts to query the ASIC for temperature, voltage or fan speed information, it will receive invalid data. Any system alerts based on the status of those parameters will not occur.

The monitoring of these three parameters is the only function affected by this erratum. The rest of the system will function normally in all other respects. Applications that do not use management software to monitor these hardware parameters are not affected by this erratum.

WORKAROUND: Power down the system and all external devices connected to it. While all external devices are still turned off, power the system on again. Turning off all external devices reduces the offset potential to a low value that allows the management ASIC to reset when power is turned on again.

STATUS: This erratum will be fixed in a future PBA revision.

SPECIFICATION CLARIFICATIONS

The Specification Clarifications listed in this section apply to the *VS440FX Motherboard Technical Product Specification* (Order Number 281812). All Specification Clarifications will be incorporated into a future version of that specification.

1. Enabling Interrupts in System Management Mode (SMM)

Section 3.8, *Advanced Power Management*, describes the use of System Management Mode by the BIOS.

System Management Mode uses its own address space. The pointers to interrupt service routines in protected mode do not necessarily point to executable interrupt service routines when the processor goes into SMM. Interrupts are disabled upon entry to SMM. Any program that wants to use interrupts during SMM must provide a valid interrupt service routine and place a pointer to it in an interrupt descriptor table before reenabling interrupts.

When the Microsoft Windows 95 operating system places an Energy Star compliant monitor in video standby mode after a period of system inactivity, it uses the motherboard BIOS to put the processor into System Management Mode. The motherboard BIOS in turn invokes the video BIOS to place the monitor into standby mode. Some video BIOSes reenable interrupts when they are called but do not ensure that a valid interrupt service routine is available. If the video BIOS then generates a hardware or software interrupt while the system is in SMM, in most cases the system will lock up.

Intel has added code to its motherboard BIOS to mask the effect of reenabling hardware interrupts without providing an interrupt service routine while in System Maintenance Mode. This workaround was implemented in BIOS revision 1.00.09.CS1.

2. Advanced Power Management (APM) Will Not Function as Expected with Universal Serial Bus (USB) Enabled

The following will be added to Section 1.7.4, *Universal Serial Bus Support* and Section 3.8, *Advanced Power Management*:

Advanced Power Management will not function as expected when a USB keyboard or mouse is used. USB activity is not monitored by the APM event counter, therefore activity from a USB keyboard or mouse will not keep the system awake or bring a system out of APM sleep mode. If a USB keyboard or mouse is being used, APM should be disabled.

*3. 64 MB SIMM*s Will Cause Performance Degradation*

The following will be added to Section 1.6, *Main Memory*:

In order to allow use of 64 MB SIMM*s, the BIOS changes to slower memory access parameters when 64MB SIMMs are detected in the system. This will result in some performance degradation if 64 MB SIMMs are installed.

4. PCI 2.1 Specification Optional Features

The following will be added to Section 1.12, *Add-in Board Expansion Connectors*:

The following optional features in the PCI 2.1 Specification are not implemented on the VS440FX motherboard:

- Cache Support Pins **SBO#** and **SDONE** (Section 2.2.7)
- **PRSNTx#** (Section 2.2.8)
- **CLKRUN#** (Section 2.2.8)
- 64 Bit Bus Extension Pins (Section 2.2.9)
- 66 MHz support (Section 2.2.8)
- JTAG/Boundary scan (Section 2.2.10)

5. Administrator and User Passwords

The following will be added to Section 3.15.12.1, *Administrative and User Access Modes*:

If an administrator password has been set, but no user password has been set, a user can create a password by entering BIOS Setup at boot by pressing the <F1> key and pressing enter at the administrator password prompt. Once in Setup, a user will be able to create a new user password.

Once defined, a user password can be cleared by either defining a new user password in Setup, or by moving the Password Clear jumper (J6D1) on the motherboard. See Section 1.13.2, *Password Clear*, for more information on how to use this jumper.

DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the *VS440FX Motherboard Technical Product Specification* (Order Number 281812). All Documentation Changes will be incorporated into a future version of that specification.

1. Change Description of Auxiliary Fan Connector for Some Motherboards

The description of the auxiliary fan connector in Section 1.11.8 applies only to motherboards with PBA revision level -5xx or higher. Earlier motherboards use the following description for that connector:

AUXILIARY FAN CONNECTOR - J9A1

Pin	Signal Name
1	Ground
2	+12V
3	Ground
4	Ground
5	+12V
6	Ground

2. Revise IO Address for Management Extension Hardware

Section 1.10, *Management Extension Hardware*, will be replaced in its entirety as follows:

The optional Management Extension Hardware provides low-cost instrumentation capabilities designed to reduce the total cost of owning a PC. The hardware implementation is a single-chip ASIC. Features include:

- An integrated temperature sensor
- Fan speed sensors for up to three fans
- Power supply voltage monitoring to detect levels above or below acceptable values
- Security switch for detecting physical intrusion, such as when the chassis lid has been removed (even when power is off). A photosensor is used as the switch.
- Remote reset capabilities from a remote peer or server through LANDesk® Client Manager, Version 3.0 and service layers (when available)

When suggested ratings for temperature, fan speed, or voltage are exceeded, an interrupt is activated.

The Management Extension circuitry connects to the ISA bus as an 8-bit I/O mapped device

The following entry will be added to Table 10, *I/O Map*:

Address (hex)	Size	Description
0290-0297	8 bytes	Management Extension Hardware

3. Add Support for 3.5 V Processors

VS440FX motherboards with the following PBA numbers and later include a header to support Pentium Pro processors that require V_{CC} of 3.5 V ± 5%:

655390-504

661105-506

663900-505

665559-502

The voltage requirement of a Pentium Pro processor is found in the column headed V_{CC} of the table *Basic 150-, 166-, 180-, and 200-Mhz Pentium® Pro Processor Identification Information* in the *Pentium® Pro Processor Specification Update* (Order Number 242689).

In order to use a 3.5 V processor in a VS440FX motherboard, a jumper must be installed between pins 1 and 2 of the header located at J4H1.

Warning: Do not install a jumper on this header if you are using a processor that does not require 3.5 V. The increased voltage supplied to the processor could damage it.

4. Revision of Section 5.1, Specifications

The following note will be added to Section 5.1, *Specifications*:

NOTE: Certain optional PCI features have not been implemented on this motherboard, see Section 1.14 for more information.

5. Revision of Section 1.7.1, 82441FX PCI Bridge and Memory Controller (PMC)

The 3rd bullet in this section will be replaced in its entirety as follows:

- Fully synchronous PCI bus interface
  - 25/30/33 MHz
  - PCI to DRAM data transfers up to or greater than 100 MB/sec
  - Up to 5 PCI bus masters in addition to the PIIX3

6. Change to Description of Serial Port Capabilities

Section 1.8.1, *Serial Ports*, will be replaced in its entirety as follows:

The motherboard has two 9-pin D-Sub serial port connectors located on the back panel. The NS16C550-compatible UARTs support data transfers at speeds up to 115.2 Kbaud.