SE440BX-3 Motherboard
Technical Product Specification

February 1999

Order Number: 726984-001

The SE440BX-3 motherboard may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the SE440BX-3 Motherboard Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the SE440BX-3 Motherboard Technical Product Specification	February 1999

This product specification applies only to standard SE440BX-3 motherboards with BIOS identifier 4S4EB3X0.86A.

Changes to this specification will be published in the SE440BX-3 Motherboard Specification Update before being incorporated into a revision of this document.

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the SE440BX-3 motherboard. It describes the standard motherboard product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the motherboard and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on this board
2	A map of the resources of the board
3	The features supported by the BIOS Setup program
4	The contents of the BIOS Setup program's menus and submenus
5	A description of the BIOS error messages, beep codes, and POST codes
6	A list of where to find information about specifications supported by the motherboard

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions which, if not observed, can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
(NxnX)	When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the motherboard, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area.
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
GB	Gigabyte (1,073,741,824 bytes)
Xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.

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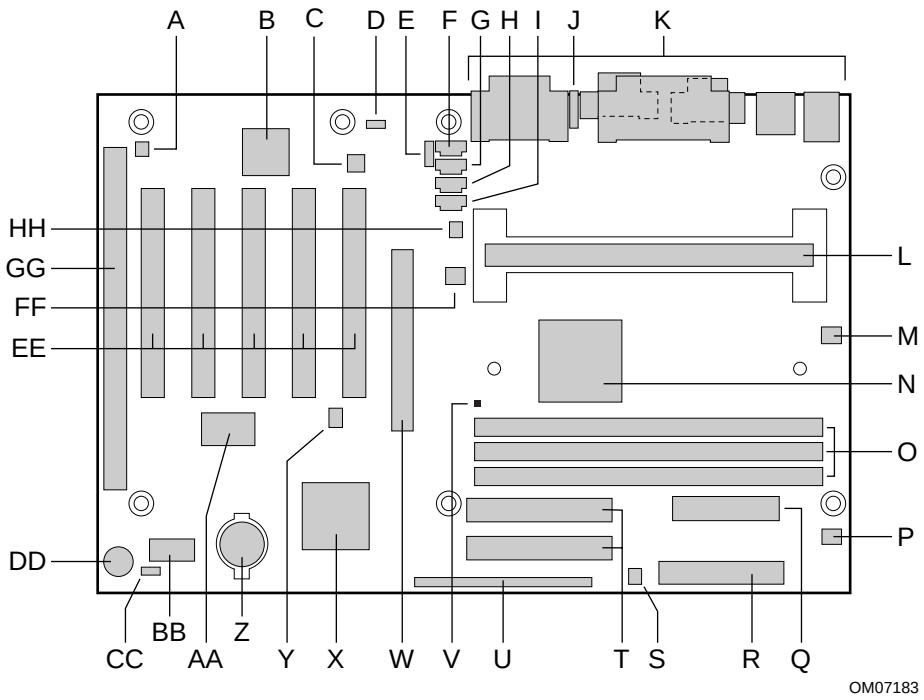
Tables

1 Motherboard Description

1.1 Overview

The SE440BX-3 motherboard's features are summarized below.

Form Factor	ATX (12 inches by 7.75 inches)
Processor	Support for one of the following processors: • Intel® Pentium® III processor with host bus frequencies of 100 MHz • Intel® Pentium® II processor with host bus frequencies of 66 MHz or 100 MHz • Intel® Celeron™ processor with host bus frequency of 66 MHz
Chipset	Intel® 82440BX AGPset, consisting of: • Intel® 82443BX PCI/AGP controller (PAC) • Intel® 82371EB PCI ISA IDE Xcelerator (PIIX4E)
Memory	• Three 168 pin dual inline memory module (DIMM) sockets • Support for up to 768 MB of 66 MHz or 100 MHz synchronous DRAM (SDRAM) • Support for error checking and correcting (ECC)
I/O Control	SMSC FDC37M707 I/O controller
Peripheral Interfaces	• Two serial ports • One parallel port • Two USB ports • Two fast IDE interfaces that support up to four IDE drives or devices • DMA support • An interface for one diskette drive
Video	One AGP slot
Speaker	Integrated 47 ohm inductor speaker
Expansion Capabilities	• Four PCI slots • One shared slot for either a PCI or an ISA add-in board
BIOS	• Intel/Phoenix BIOS • Support for SMBIOS, ACPI, APM, and Plug and Play (see Section 6.2 for specification compliance levels)



A	Wake on Ring connector (optional)	R	Diskette drive connector
B	Yamaha YMF724 (DS1) PCI audio controller (optional)	S	SCSI LED connector (optional)
C	Analog Devices AD1819A SoundPort† Codec (optional)	T	IDE connectors
D	Wake on LAN† technology connector (optional)	U	Front panel connectors
E	Legacy CD-ROM audio connector (optional)	V	Standby Power LED (optional)
F	CD-ROM Line In audio connector (optional)	W	Accelerated Graphics Port (AGP) connector
G	Telephony connector (optional)	X	Intel 82371EB PCI ISA IDE Xcelerator (PIIX4E)
H	Auxiliary Line In audio connector (optional)	Y	PC/PCI connector
I	Video Line In audio connector (optional)	Z	Battery
J	Diagnostic LEDs (optional)	AA	SMSC FDC37M707 Super I/O controller
K	Back panel connectors	BB	Flash BIOS
L	242-contact slot connector	CC	Configuration jumper block
M	Active fan heatsink (fan 2) connector	DD	Integrated speaker
N	Intel 82443BX PCI/AGP controller	EE	PCI connectors
O	DIMM sockets	FF	Fan 3 connector
P	Fan 1 connector	GG	ISA connectors
Q	Power supply connector	HH	Chassis intrusion connector (optional)

Figure 1. Motherboard Components

The following are manufacturing options. Not all manufacturing options are available in all marketing channels. Please contact your Intel representative to determine what manufacturing options are available to you.

Manufacturing Options

Audio Subsystem	AC '97 compatible • Yamaha YMF724 (DS-1) PCI audio controller • Analog Devices AD1819A SoundPort Codec
Hardware Monitor Subsystem	• Management Level 3 support • Two fan sense inputs used to monitor fan activity • Two pin header security feature for intrusion detection • Voltage sense to detect out of range values
Wake on LAN Technology Connector	Support for system wake up using an add-in network interface card with remote wake up capability
Wake on Ring Connector	Support for system wake up using an add-in telephony device, such as a modem
SCSI LED Connector	Allows add-in SCSI controllers to use the same LED as the onboard front-panel LED
Enhanced Diagnostics	Embedded diagnostics and LED display that supplement beep codes during POST
Instantly Available	• S3 sleep state support with Suspend-to-RAM • Less than 5 W power consumption

1.2 Microprocessor

The motherboard supports a single Pentium III processor, Pentium II processor, or Celeron processor. The processor's VID pins automatically program the voltage regulator on the motherboard to the required processor voltage. In addition, the host bus frequency (66 MHz and 100 MHz) is automatically selected. The processor connects to the motherboard through a 242-contact slot connector. The processor must be secured by a retention mechanism attached to the motherboard.

⚠ CAUTION

Processors with a 100 MHz host bus should be used only with 100 MHz SDRAM; the motherboard will not operate reliably if a processor with a 100 MHz host bus is paired with 66 MHz SDRAM. However, processors with a 66 MHz host bus can be used with either 66 MHz or 100 MHz SDRAM.

The motherboard supports the processors listed in Table 1.

Table 1. Supported Processors

Processor Type	Processor Speed (in MHz)	Host Bus Frequency (in MHz)	Level 2 Cache (in KB)
Pentium III processor	450 500	100 100	512 512
Pentium II processor	233 266 300 333 350 400 450	66 66 66 66 100 100 100	512 512 512 512 512 512 512
Celeron processor	266 300 300A 333 366 400	66 66 66 66 66 66	0 0 128 128 128 128

1.2.1 Second Level Cache

The second-level cache for the Pentium III processor and the Pentium II processor includes 512 KB of synchronous pipelined burst static RAM (PBSRAM) and tag RAM. All supported onboard memory can be cached.

Intel Celeron processors 300A, 333, 366, and 400 MHz include 128K of integrated L2 cache. All supported onboard memory can be cached.

1.2.2 Microprocessor Upgrades

The motherboard can be upgraded with processors listed in Table 1. When upgrading the processor, use the BIOS configuration mode to change the processor speed (see Section 1.13).

1.3 Memory

1.3.1 Main Memory

The motherboard has three DIMM sockets. SDRAM can be installed in one, two, or three sockets. EDO DIMMs are not supported. Using the serial presence detect (SPD) data structure, programmed into an E^2PROM on the DIMM, the BIOS can determine the SDRAM's size and speed. Minimum memory size is 16 MB; maximum memory size is 768 MB. Memory size and speed can vary between sockets.

The motherboard supports the following memory features:

- 168-pin DIMMs with gold-plated contacts
- 66 or 100 MHz SDRAM
- Non-ECC (64-bit) and ECC (72-bit) memory
- 3.3 V memory only
- Unbuffered single- or double-sided DIMMs in the following common sizes:

DIMM Capacity	Non-ECC DIMM Organization*	SDRAM Density	SDRAM Organization	Number of SDRAMs
16 MB	2M X 64	16 Mbit	1M X 16	8
16 MB	2M X 64	16 Mbit	2M X 8	8
16 MB	2M X 64	64 Mbit	2M X 32	2
32 MB	4M X 64	16 Mbit	2M X 8	16**
32 MB	4M X 64	64 Mbit	2M X 32	4
32 MB	4M X 64	64 Mbit	4M X 16	4
64 MB	8M X 64	64 Mbit	4M X 16	8
64 MB	8M X 64	64 Mbit	8M X 8	8
128 MB	16M X 64	64 Mbit	8M X 8	16**
256 MB	32M x 64	128 Mbit	16M x8	16**

* ECC DIMM organization is X 72 and additional components are used on each side of the DIMM.

** If the number of SDRAMs is greater than nine, the DIMM will be double sided.

NOTE

Processors with 100 MHz host bus should be paired only with 100 MHz SDRAM. Processors with 66 MHz host bus can be paired with either 66 MHz or 100 MHz SDRAM.

CAUTION

To be fully compliant with all applicable Intel® SDRAM memory specifications, the motherboard should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. If your memory modules do not support SPD, you will see a notification to this effect on the screen at power up. The BIOS will attempt to configure the memory controller for normal operation. However, DIMMs may not function at the determined frequency. See Section 6.2 for information about the specifications Serial Presence Detect specification.

NOTE

All memory components and DIMMs used with the SE440BX-3 motherboard should comply with the PC SDRAM specifications. These include: the PC SDRAM Specification (memory component specific), the PC100 SDRAM Component Testing Summary, and the PC Unbuffered DIMM Specification. See Section 6.2 for information about these specifications.

1.3.2 ECC Memory

ECC memory detects multiple-bit errors and corrects single-bit errors. When ECC memory is installed, the BIOS supports both ECC and non-ECC mode. ECC mode is enabled in the Setup program. The BIOS automatically detects if ECC memory is installed and provides the Setup option for selecting ECC mode. If any non-ECC memory is installed, the Setup option for ECC configuration does not appear and ECC operation is not available.

1.4 Chipset

The Intel® 440BX chipset includes a Host-PCI bridge integrated with both an optimized DRAM controller and an AGP interface. The I/O subsystem of the 440BX is based on the PIIX4E, which is a highly integrated PCI-ISA/IDE Accelerator Bridge. This chipset consists of the Intel 82443BX PCI/AGP controller (PAC) and the Intel 82371EB PCI/ISA IDE Xcelerator (PIIX4E) bridge chip.

1.4.1 Intel® 82443BX PCI/AGP Controller (PAC)

The PAC provides bus-control signals, address paths, and data paths for transfers between the processor's host bus, PCI bus, the AGP, and main memory. The PAC features:

- Processor interface control
  - Support for processor host bus frequencies of 100 MHz or 66 MHz
  - 32-bit addressing
  - Desktop Optimized GTL+ compliant host bus interface
- Integrated DRAM controller, with support for:
  - +3.3 V only DIMM DRAM configurations
  - Up to three double sided DIMMs
  - 100 MHz or 66 MHz SDRAM
  - DIMM serial presence detect via SMBus interface
  - 16- and 64-Mbit devices with 2 K, 4 K, and 8 K page sizes
  - x 8, x 16, and x 32 DRAM widths
  - SDRAM 64-bit data interface with ECC support
  - Symmetrical and asymmetrical DRAM addressing

- AGP interface
  - Complies with the AGP specification (see Section 6.2 for specification information)
  - Support for +3.3 V AGP-66/133 devices
  - Synchronous coupling to the host-bus frequency
- PCI bus interface
  - Complies with the PCI specification (see Section 6.2 for specification information)
  - Asynchronous coupling to the host-bus frequency
  - PCI parity generation support
  - Data streaming support from PCI-to-DRAM
  - Support for five PCI bus masters in addition to the host and PCI-to-ISA I/O bridge
  - Support for concurrent host, AGP, and PCI transactions to main memory
- Data buffering
  - DRAM write buffer with read-around-write capability
  - Dedicated host-to-DRAM, PCI0-to-DRAM, and PCI1/AGP-to-DRAM read buffers
  - AGP dedicated inbound/outbound FIFOs (133/66 MHz), used for temporary data storage
- Power management functions
  - Support for system suspend/resume (DRAM and power-on suspend)
  - Compliant with ACPI power management (see Section 6.2 for specification information)
- SMBus support for desktop management functions
- Support for system management mode (SMM)

1.4.2 Intel® 82371EB PCI ISA IDE Xcelerator (PIIX4E)

The PIIX4E is a multifunction PCI device implementing the PCI-to-ISA bridge, PCI IDE functionality, USB host/hub functionality, and enhanced power management. The PIIX4E features:

- Multifunction PCI-to-ISA bridge
  - Support for the PCI bus at 33 MHz
  - Complies with the PCI specification
  - Full ISA bus support
- USB controller
  - Two USB ports (see Section 6.2 for specification information)
  - Support for legacy keyboard and mouse
  - Support for UHCI interface
- Integrated dual-channel enhanced IDE interface
  - Support for up to four IDE devices
  - PIO Mode 4 transfers at up to 16 MB/sec
  - Support for Ultra DMA/33 synchronous DMA mode transfers at up to 33 MB/sec
  - Bus master mode with an 8 x 32-bit buffer for bus master PCI IDE burst transfers

- Enhanced DMA controller
  - — Two 8237-based DMA controllers
  - — Support for PCI DMA with three PC/PCI channels and distributed DMA protocols
- Interrupt controller based on 82C59
  - — Support for 15 interrupts
  - — Programmable for edge/level sensitivity
- Power management logic
  - — Sleep/resume logic
  - — Support for wake-on-modem, Wake on LAN technology, and wake on PME
  - — Support for ACPI (see Section 6.2 for specification information)
- Real-Time Clock
  - — 256-byte battery-backed CMOS SRAM
  - — Includes date alarm
- 16-bit counters/timers based on 82C54

1.4.3 Accelerated Graphics Port (AGP)

The motherboard has one AGP connector for high-performance graphics add-in cards. AGP, while based on the *PCI Local Bus Specification, Rev. 2.1*, is independent of the PCI bus and is intended for exclusive use with graphical display devices. AGP overcomes certain limitations of the PCI bus related to handling a large amount of graphics data with the following features:

- Pipelined memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for near 100 percent bus efficiency
- AC timing for 133 MHz data transfer rates, allowing real data throughput in excess of 500 MB/sec

For more information on the AGP, please refer to the *Accelerated Graphics Port Interface Specification* listed in Section 6.2.

1.4.4 Universal Serial Bus (USB)

The motherboard has two USB ports; one USB peripheral can be connected to each port. For more than two USB devices, an external hub can be connected to either port. The motherboard fully supports the universal host controller interface (UHCI) and uses UHCI-compatible software drivers. See Section 6.2 for information about the USB specification. USB features include:

- Self-identifying peripherals that can be plugged in while the computer is running
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error-handling and fault-recovery mechanisms built into the protocol

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device or a low-speed USB device is attached to the cable. Use shielded cable that meets the requirements for a full-speed USB device.

1.4.5 IDE Support

The motherboard has two independent bus-mastering PCI IDE interfaces. These interfaces support:

- ATAPI devices (such as CD-ROM drives)
- ATA devices using the transfer modes mentioned in Table 56 on page 80

The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The BIOS automatically detects the IDE device transfer rate and translation mode.

The motherboard also supports laser servo (LS-120) drives. LS-120 technology allows the user to perform read/write operations to LS-120 (120 MB) and conventional 1.44 MB and 720 KB diskettes. LS-120 drives are ATAPI-compatible and connect to the motherboard's IDE interface. (LS-120 drives are also available with SCSI and parallel port interfaces.) Some versions of Windows† 95, Windows 98, and Windows NT† operating systems recognize the LS-120 drive as a bootable device in both 120 MB and 1.44 MB mode.

Connection of an LS-120 drive and a standard 3.5-inch diskette drive is allowed. The LS-120 drive can be configured as a boot device if selected as Drive A in the BIOS setup program.

NOTE

If you connect an LS-120 drive to an IDE connector and configure it as the "boot" drive and configure a standard 3.5-inch diskette drive as a "B" drive, the standard diskette drive is not seen by the operating system. When the LS-120 drive is configured as the "boot" device, the system will recognize it as both the A and B drive.

1.4.6 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock is compatible with DS1287 and MC146818 components. The clock provides a time-of-day clock and a multicentury calendar with alarm features and century rollover. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

The time, date, and CMOS values can be specified in the Setup program. The CMOS values can be returned to their defaults by using the Setup program.

NOTE

The recommended method of accessing the date in systems with Intel® motherboards is indirectly from the Real Time Clock (RTC) via the BIOS. The BIOS on Intel motherboards and baseboards contains a century checking and maintenance feature that checks the least two significant digits of the year stored in the RTC during each BIOS request (INT 1Ah) to read the date and, if less than 80 (i.e., 1980 is the first year supported by the PC), updates the century byte to 20. This feature enables operating systems and applications using the BIOS date/time services to reliably manipulate the year as a four-digit value.

For more information on proper date access in systems with Intel motherboards please see http://support.intel.com/procs/support/year2000/status/motherboard paper.htm

A coin-cell battery powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the 3.3 V standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 V applied.

1.5 I/O Interface Controller

The FDC37M707 I/O controller from SMSC is an ISA Plug and Play-compatible, multifunctional I/O device that provides the following features (see Section 6.2 for Plug and Play specification information):

- Two serial ports
- Interface for one diskette drive
- Three-mode diskette drive support (driver required)
- FIFO support on both serial and diskette drive interfaces
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- PS/2†-style mouse and keyboard interfaces
- Support for serial IRQ packet protocol
- Intelligent management, including:
  - — Shadowed write-only registers for ACPI compliance
  - — Programmable wake up event interface

The BIOS Setup program provides configuration options for the I/O controller.

1.5.1 Serial Ports

The motherboard has two 9-pin D-Sub serial port connectors located on the back panel. The NS16C550-compatible UARTs support data transfers at speeds up to 115.2 Kbits/sec with BIOS support.

1.5.2 Parallel Port

The connector for the multimode bi-directional parallel port is a 25-pin D-Sub connector located on the back panel of the motherboard. In the Setup program, there are four options for parallel port operation:

- Output Only (AT†-compatible mode).
- Bi-directional (PS/2 compatible mode).
- EPP (a high-speed bi-directional mode). A driver from the peripheral manufacturer is required for operation. See Section 6.2 for EPP compatibility.
- ECP (a high-speed bi-directional mode).

1.5.3 Diskette Drive Controller

The I/O controller is software compatible with the 82077 diskette drive controller and supports both PC-AT† and PS/2 modes. In the Setup program, the diskette drive interface can be configured for the following diskette drive capacities and sizes:

- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.44/1.25 MB, 3.5-inch
- 2.88 MB, 3.5-inch

NOTE

The I/O controller supports 1.2 MB, 3.5-inch diskette drives, but a special driver is required is for this type of drive (three-mode).

1.5.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel of the motherboard. The +5 V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, reestablishes the connection after an over-current condition is removed.

NOTE

The mouse and keyboard can be plugged into either PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains code which provides the traditional keyboard and mouse control functions, and also supports Power On/Reset password protection. A Power On/Reset password can be specified in the BIOS Setup program.

1.5.5 Infrared Support

On the front panel I/O connector, there are five pins that support the Hewlett Packard HSDL-1000 compatible infrared (IR) transmitters and receivers. In the Setup program, Serial Port B can be directed to a connected IR device. (In this case, the Serial Port B connector on the back panel cannot be used.) The IR connection can be used to transfer files to or from portable devices like laptops, PDAs, and printers. The Infrared Data Association (IrDA†) specification supports data transfers of 115 Kbits/sec at a distance of 1 meter. See Section 6.2 for information about the IrDA specification.

1.6 Audio Subsystem (Optional)

The SE440BX-3 motherboard has an optional Audio Codec ’97 (AC ’97) compatible audio subsystem, which consists of the following components:

- Analog Devices AD1819A SoundPort Codec
- Yamaha YMF724 (DS1) PCI audio controller
- Audio connectors

1.6.1 Analog Devices AD1819A SoundPort Codec

The analog codec features:

- 16-bit stereo full-duplex codec with up to 48 kHz sampling rate
- Variable 7 kHz to 48 kHz sampling rate with 1 Hz resolution
- Phat† 3D stereo enhancement

1.6.2 Yamaha YMF724 (DS-1) PCI Audio Controller

The audio controller features:

- *PCI Local Bus Specification*, rev. 2.1 compliant
- PC 97/PC 98 compliant
- *PCI Bus Power Management Interface Specification*, rev. 1.0 compliant
- PCI bus master for PCI audio
- PC/PCI support for legacy DMAC emulation
- Serialized IRQ support
- 64-voice hardware wavetable synthesis
- Sound Blaster Pro†, Roland MPU-401 UART-mode MIDI, and joystick compatibility

1.6.3 Audio Connectors

The audio connectors include the following:

- Stacked backpanel connectors with Line In, Line Out, Mic, and MIDI/game port
- Optional legacy CD-ROM audio connector
- Optional CD-ROM Line In audio connector (black)
- Optional telephony connector (green)
- Optional auxiliary Line In audio connector (white)
- Optional video Line In audio connector (blue)

See Sections 1.12.1 and 1.12.2 for the location and pinouts of the audio connectors.

1.6.3.1 Legacy CD-ROM Audio Connector

A 1 x 4 pin connector (J1F2) is available for connecting an internal Legacy CD-ROM drive to the audio mixer. The connector is designed for use with cables that are compatible with Legacy CD-ROM drives.

1.6.3.2 CD-ROM Line In Audio Connector

A 1 x 4-pin ATAPI-style connector (J1F1) is available for connecting an internal CD-ROM drive to the audio mixer. The connector is designed for use with cables that are compatible with ATAPI CD-ROM drives.

1.6.3.3 Telephony Connector

A 1 x 4-pin ATAPI-style connector (J2F1) is available for connecting the monaural audio signals of an internal telephony device to the audio subsystem. A monaural audio-in and audio-out signal interface is necessary for telephony applications such as speakerphones, faxmodems, and answering machines.

1.6.3.4 Auxiliary Line In Audio Connector

A 1 x 4-pin ATAPI-style Line In connector (J2F2) is available for connecting the left and right channel signals of an internal audio device to the audio subsystem. An audio-in signal interface of this type is necessary for applications such as TV tuners.

1.6.3.5 Video Line In Audio Connector

A 1 x 4 pin ATAPI-style connector (J2F3) is available for connecting the left and right channel signals of an internal audio device.

1.6.4 Audio Drivers and Utilities

Audio software and utilities are available from Intel's World Wide Web site (see Section 6.1).

1.7 Hardware Monitor Subsystem (Optional)

The features of the hardware monitor subsystem include:

- Management level 3 support
- Voltage sense (+12 V, -12 V, +5 V, +3.3 V, +1.5 V, and VCCP) to detect out of range values
- Chassis intrusion detection (a 2 pin header is provided to connect security feature)
- Two fan sense inputs can be used to monitor fan activity (3 pin fan headers include +12 V (fan control), ground, and tachometer/sense pins)
- An integrated ambient temperature sensor
- Fan speed sensors, which monitor the fan 1 and fan 2 connectors (see Figure 5 for the location of these connectors on the motherboard)
- Power supply voltage monitoring to detect levels above or below acceptable values

When suggested ratings for temperature, fan speed, or voltage are exceeded, an interrupt is activated. The hardware monitor component connects to the SMBus.

The optional hardware monitor subsystem supports a chassis security feature that detects if the chassis cover is removed and sounds an alarm (through the onboard piezoelectric speaker or PC chassis speaker, if either is present). For the chassis intrusion circuit to function, the chassis' power supply must be connected to AC power. The security feature uses a mechanical switch on the chassis that is attached to a 1 x 2 pin connector (J3F1). The mechanical switch is closed for normal computer operation. See Section 1.12.2 for the location and pinouts of the chassis intrusion connector.

1.8 Wake on LAN Technology (Optional)

Wake on LAN technology enables remote wakeup of the computer through a network. Wake on LAN technology requires a PCI add-in network interface card (NIC) with remote wakeup capabilities. The remote wakeup connector on the NIC must be connected to the onboard Wake on LAN technology connector. The NIC monitors network traffic at the MII interface; upon detecting a Magic Packet†, the NIC asserts a wakeup signal that powers up the computer. To access this feature use the Wake on LAN technology connector. See Section 1.12.2 for the location and pinouts of the Wake on LAN technology connector.

⚠ CAUTION

For Wake on LAN, the 5-V standby line for the power supply must be capable of delivering +5 V ±5 % at a minimum of 720 mA. Failure to provide adequate standby current when implementing Wake on LAN can damage the power supply.

1.9 Wake on Ring/Resume on Ring Technologies

This section describes two technologies that enable telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal) and the power management mode being used (APM or ACPI). For information about APM and ACPI, refer to Section 3.4.

NOTE

Wake on ring and resume on ring technologies require the support of an operating system that provides full ACPI functionality.

1.9.1 Wake on Ring Technology

The operation of Wake on Ring can be summarized as follows:

- Powers up the computer from either the APM soft-off mode or the ACPI S5 state
- Requires two calls to access the computer:
  - The first call powers up the computer
  - The second call enables access (if the appropriate software is loaded)
- Detects an incoming call differently for external as opposed to internal modems:
  - For external modems, motherboard hardware monitors the ring indicate (RI) input of serial port A (serial port B does not support this feature)
  - For internal modems, a cable must be routed from the modem to the optional Wake on Ring connector (see Figure 5)

1.9.2 Resume on Ring Technology

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from either the APM sleep mode or the ACPI S1 state
- Requires only one call to access the computer
- Detects incoming call similarly for external and internal modems; does not use the Wake on Ring connector
- Requires modem interrupt be unmasked for correct operation

1.10 Enhanced Diagnostics (Optional)

The enhanced diagnostics option consists of a hardware decoder and four dual-colored LEDs located on the backpanel (see Figure 2). As the system boots, the BIOS tests specific areas of the motherboard. If the BIOS hangs during one of these tests, the state of the diagnostic LEDs indicates which BIOS operation was in progress when the BIOS hung. The enhanced diagnostics option requires no modifications to the chassis other than the I/O shield (see Figure 11). Table 2 lists the valid states of the diagnostic LEDs.

Table 2. Diagnostic LEDs States

LED	State	Description	LED	State	Description
1 2 3 4	Amber Amber Amber Amber	Power on, starting the BIOS	1 2 3 4	Amber Green Amber Green	Testing video
1 2 3 4	Amber Amber Amber Green	Recovery mode	1 2 3 4	Amber Green Green Amber	Initializing the IDE bus
1 2 3 4	Amber Amber Green Amber	Testing the processor, cache, etc.	1 2 3 4	Amber Green Green Green	Initializing the USB
1 2 3 4	Amber Amber Green Green	Testing memory	1 2 3 4	Green Green Green Green	Booting the operating system
1 2 3 4	Amber Green Amber Amber	Initializing the PCI bus			

Note: Other states are reserved for future use.

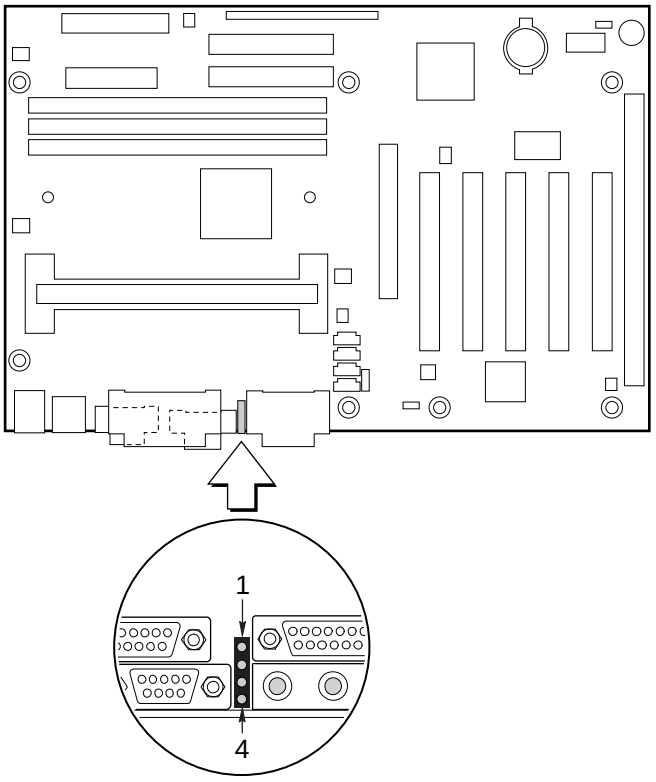


Figure 2. Diagnostic LEDs

1.11 Instantly Available Technology (Optional)

Instantly Available technology enables the board to enter the ACPI S3 (Suspend-to-RAM) sleep state. While in the S3 sleep state, the system will appear to be off. When signaled by a wake up device or event, the system quickly returns to its last known wake state. Table 47 lists the devices and events that can wake the computer from the S3 state.

The board supports the *PCI Bus Power Management Interface Specification* and the 3.3V Aux ECR. For information on the versions of this specification, see Section 6.2. Add-in boards that support this specification can participate in power management and can be used to wake the system.

The optional standby power LED, located between the DIMM sockets and processor connector (see Figure 1), provides an indication that power is still present to the DIMM sockets and PCI slots, even when the system appears to be off.

CAUTION

When the board is installed in a chassis, it is necessary to remove the chassis cover to see the state of the LED. Disconnect the power cord to the system prior to removing the chassis cover. Failure to do so could damage the motherboard, any installed memory, PCI add-in boards, or the power supply.

NOTE

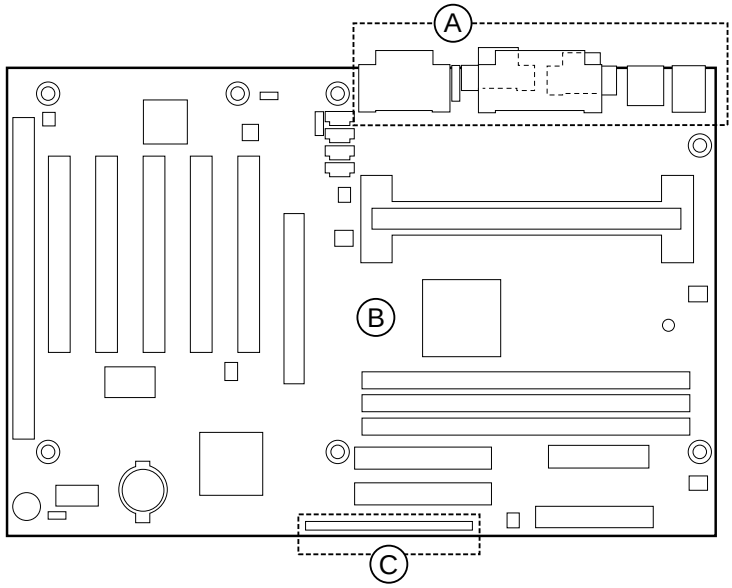
To support Instantly Available technology, the power supply must be capable of providing enough stand-by current from the 5 V stand-by source. 720 mA is usually sufficient, but this depends on wakeup devices supported and manufacturing options.

1.12 Connectors

Figure 3 shows the location of the motherboard connectors.

CAUTION

Only the back panel connectors of this motherboard have overcurrent protection The internal motherboard connectors are not overcurrent protected and should connect only to devices inside the computer chassis such as fans and internal peripherals. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.



A Back panel connectors (see page 29)

B Midboard connectors (see page 33)

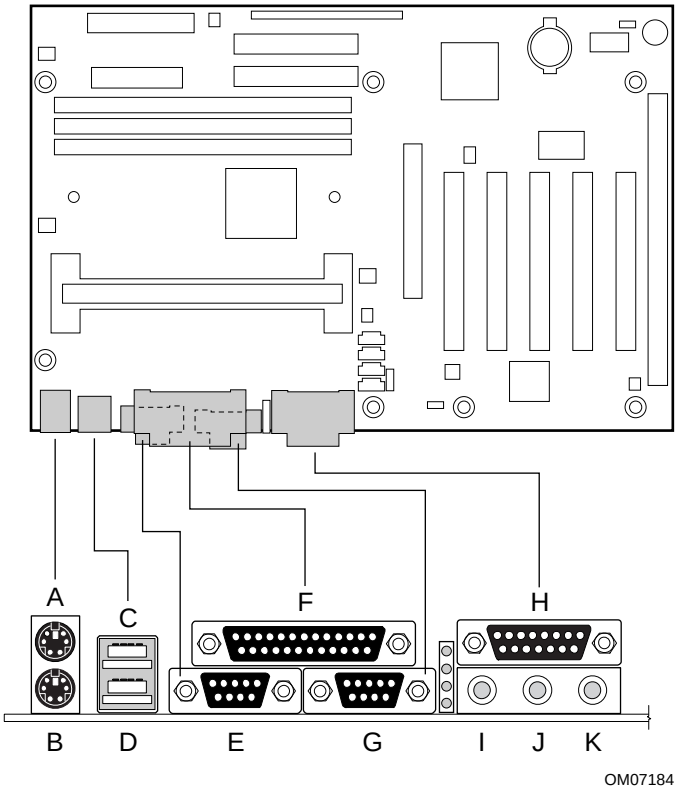
C Front panel connectors (see page 41)

Figure 3. Connector Groups

1.12.1 Back Panel Connectors

Figure 4 shows the location of the back panel connectors, which include:

- PS/2-keyboard and mouse connectors
- Two USB connectors
- One parallel port
- Two serial ports
- MIDI/game port (optional)
- Optional external audio jacks: Line Out, Line In, and Mic In



A	PS/2 keyboard or mouse	G	Serial Port B
B	PS/2 keyboard or mouse	H	MIDI/game Port (optional)
C	USB Port 1	I	Audio Line Out (optional)
D	USB Port 0	J	Audio Line In (optional)
E	Serial Port A	K	Audio Mic In (optional)
F	Parallel Port		

Figure 4. Back Panel Connectors

Table 3. PS/2 Keyboard/Mouse Connectors

Pin	Signal Name
1	Data
2	No connect
3	Ground
4	+5 V (fused)
5	Clock
6	No connect

Table 4. USB Connectors

Pin	Signal Name
1	+5 V (fused)
2	USBP0# [USBP1#]
3	USBP0 [USBP1]
4	Ground

Signal names in brackets ([ ]) are for USB Port 1.

Table 5. Serial Port Connectors

Pin	Signal Name
1	DCD
2	Serial In#
3	Serial Out#
4	DTR
5	Ground
6	DSR
7	RTS
8	CTS
9	RI

Table 6. Parallel Port Connector

Pin	Signal Name	Pin	Signal Name
1	Strobe#	14	Auto Feed#
2	Data bit 0	15	Fault#
3	Data bit 1	16	INIT#
4	Data bit 2	17	SLCT IN#
5	Data bit 3	18	Ground
6	Data bit 4	19	Ground
7	Data bit 5	20	Ground
8	Data bit 6	21	Ground
9	Data bit 7	22	Ground
10	ACK#	23	Ground
11	Busy	24	Ground
12	Error	25	Ground
13	Select		

Table 7. MIDI/Game Port Connector

Pin	Signal Name	Pin	Signal Name
1	+5 V (fused)	9	+5 V (fused)
2	GP4 (JSBUT0)	10	GP6 (JSBUT2)
3	GP0 (JSX1)	11	GP2 (JSX2)
4	Ground	12	MIDI-OUT
5	Ground	13	GP3 (JSY2)
6	GP1 (JSY1)	14	GP7 (JSBUT3)
7	GP5 (JSBUT1)	15	MIDI-IN
8	+5 V (fused)		

Table 8. Audio Line Out Connector

Pin	Signal Name
Sleeve	Ground
Tip	Audio Left Out
Ring	Audio Right Out

Table 9. Audio Line In Connector

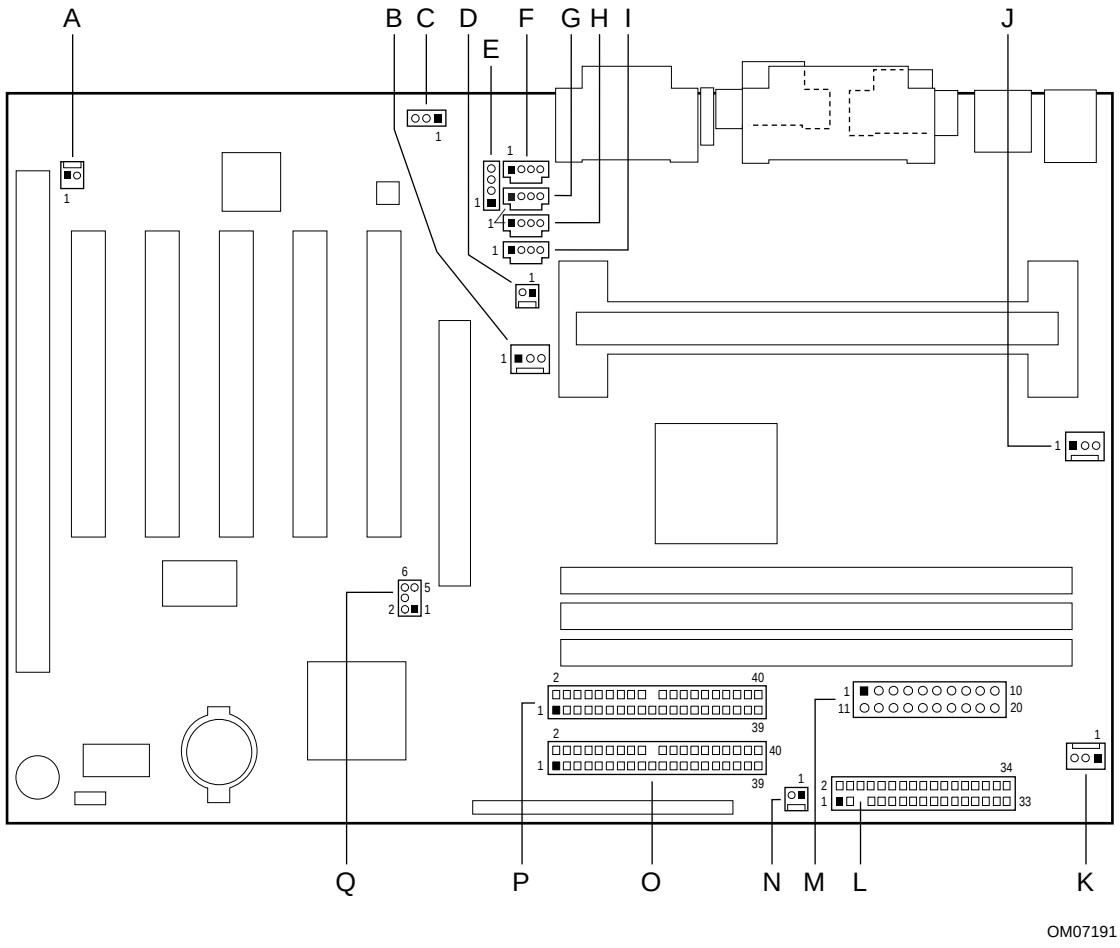
Pin	Signal Name
Sleeve	Ground
Tip	Audio Left In
Ring	Audio Right In

Table 10. Audio Mic In Connector

Pin	Signal Name
Sleeve	Ground
Tip	Mono In
Ring	Electret Bias Voltage

1.12.2 Midboard Connectors

Figure 5 shows the location of the midboard I/O connectors.



A	Optional Wake on Ring (J1A1)	J	Active fan heatsink (J4M1) (fan 2)
B	Fan 3 (J3F2)	K	Fan 1 (J7M1)
C	Optional Wake on LAN technology (J1E1)	L	Diskette drive (J8K1)
D	Optional chasis intrusion (J3F1)	M	Power supply (J7L1)
E	Optional legacy CD-ROM audio (J1F2)	N	Optional SCSI LED (J8J1)
F	Optional CD-ROM Line In audio (J1F1)	O	Primary IDE (J8G1)
G	Optional telephony (J2F1)	P	Secondary IDE (J7G1)
H	Optional auxiliary Line In audio (J2F2)	Q	PC/PCI (J6D1)
I	Optional video Line In audio (J2F3)		

Figure 5. Midboard I/O Connectors

Table 11. Optional Wake on Ring Connector (J1A1)

Pin	Signal Name
1	Ground
2	RINGA#

Table 12. Fan 3 Connector (J3F2)

Pin	Signal Name
1	Ground
2	+12 V
3	Ground

Table 13. Optional Wake on LAN Technology Connector (J1E1)

Pin	Signal Name
1	+5 VSB
2	Ground
3	WOL

Table 14. Optional Chassis Intrusion Connector (J3F1)

Pin	Signal Name
1	Ground
2	CHS_SEC

Table 15. Optional Legacy CD-ROM Audio Connector (J1F2)

Pin	Signal Name
1	Ground
2	CD_IN-Left
3	Ground
4	CD_IN-Right

Table 16. Optional CD-ROM Line In Audio Connector (J1F1) (black)

Pin	Signal Name
1	CD_IN-Left
2	Ground
3	Ground
4	CD_IN-Right

Table 17. Optional Telephony Connector (J2F1) (green)

Pin	Signal Name
1	Audio In (monaural)
2	Ground
3	Ground
4	Mic pre-amp out (to modem)

Table 18. Optional Auxiliary Line In Audio Connector (J2F2) (white)

Pin	Signal Name
1	Left Line In
2	Ground
3	Ground
4	Right Line In (monaural)

Table 19. Optional Video Line In Audio Connector (J2F3) (blue)

Pin	Signal Name
1	Left Line In
2	Ground
3	Ground
4	Right Line In

Table 20. Active Fan Heatsink * (Fan 2) (J4M1)

Pin	Signal Name
1	Ground
2	FAN_CTRL (+12 V)
3	FAN_SEN**

* Recommended for use with processors with an active fan heatsink.

** If the optional hardware monitor is not installed, pin 3 is ground.

Table 21. Fan 1 Connector (J7M1)

Pin	Signal Name
1	Ground
2	FAN_CTRL (+12 V)
3	FAN_SEN*

* If the optional hardware monitor is not installed, pin 3 is ground.

Table 22. Diskette Drive Connector (J8K1)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	FDINDX# (Index)
9	Ground	10	FDM00# (Motor Enable A)
11	Ground	12	No connect
13	Ground	14	FDDS0# (Drive Select A)
15	Ground	16	No connect
17	No Connect	18	FDDIR# (Stepper Motor Direction)
19	Ground	20	FDSTEP# (Step Pulse)
21	Ground	22	FDWD# (Write Data)
23	Ground	24	FDWE# (Write Enable)
25	Ground	26	FDTRK0# (Track 0)
27	No Connect	28	FDWPD# (Write Protect)
29	Ground	30	FDRDATA# (Read Data)
31	Ground	32	FDHEAD# (Side 1 Select)
33	Ground	34	DSKCHG# (Diskette Change)

Table 23. PCI IDE Connectors (J8G1 - primary, J7G1 - secondary)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	P_ALE (Cable Select pullup)
29	DDACK0# [DDACK1#]	30	Ground
31	IRQ 14 [IRQ 15]	32	Reserved
33	Address 1	34	Reserved
35	Address 0	36	Address 2
37	Chip Select 1P# [Chip Select 1S#]	38	Chip Select 3P# [Chip Select 3S#]
39	Activity#	40	Ground

NOTE: Signal names in brackets ([ ]) are for the secondary IDE connector.

Table 24. Accelerated Graphics Port (J4E1)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	+12V	B1	No Connect	A34	Vcc3.3	B34	Vcc3.3
A2	No Connect	B2	Vcc	A35	AD22	B35	AD21
A3	Reserved	B3	Vcc	A36	AD20	B36	AD19
A4	No Connect	B4	No Connect	A37	Ground	B37	Ground
A5	Ground	B5	Ground	A38	AD18	B38	AD17
A6	INTA#	B6	INTB#	A39	AD16	B39	C/BE2#
A7	RST#	B7	CLK	A40	Vcc3.3	B40	Vcc3.3
A8	GNT1#	B8	REQ#	A41	FRAME#	B41	IRDY#
A9	Vcc3.3	B9	Vcc3.3	A42	Reserved	B42	+3.3 V aux
A10	ST1	B10	ST0	A43	Ground	B43	Ground
A11	Reserved	B11	ST2	A44	Reserved	B44	Reserved
A12	PIPE#	B12	RBF#	A45	Vcc3.3	B45	Vcc3.3
A13	Ground	B13	Ground	A46	TRDY#	B46	DEVSEL#
A14	No Connect	B14	No Connect	A47	STOP#	B47	Vcc3.3
A15	SBA1	B15	SBA0	A48	PME#	B48	PERR#
A16	Vcc3.3	B16	Vcc3.3	A49	Ground	B49	Ground
A17	SBA3	B17	SBA2	A50	PAR	B50	SERR#
A18	Reserved	B18	SB_STB	A51	AD15	B51	C/BE1#
A19	Ground	B19	Ground	A52	Vcc3.3	B52	Vcc3.3
A20	SBA5	B20	SBA4	A53	AD13	B53	AD14
A21	SBA7	B21	SBA6	A54	AD11	B54	AD12
A22	Key	B22	Key	A55	Ground	B55	Ground
A23	Key	B23	Key	A56	AD9	B56	AD10
A24	Key	B24	Key	A57	C/BE0#	B57	AD8
A25	Key	B25	Key	A58	Vcc3.3	B58	Vcc3.3
A26	AD30	B26	AD31	A59	Reserved	B59	AD_STB0
A27	AD28	B27	AD29	A60	AD6	B60	AD7
A28	Vcc3.3	B28	Vcc3.3	A61	Ground	B61	Ground
A29	AD26	B29	AD27	A62	AD4	B62	AD5
A30	AD24	B30	AD25	A63	AD2	B63	AD3
A31	Ground	B31	Ground	A64	Vcc3.3	B64	Vcc3.3
A32	Reserved	B32	AD_STB1	A65	AD0	B65	AD1
A33	C/BE3#	B33	AD23	A66	SMB0	B66	SMB1

1.12.2.1 SCSI LED Connector (Optional)

The SCSI LED connector is a 1 x 2-pin connector (J8J1) that allows add-in SCSI controllers to use the same LED as the onboard front-panel LED. This connector can be connected to the LED output of the add-in controller card. The LED will indicate when data is being read or written using the add-in controller.

Table 25. SCSI LED Connector (J8J1)

Pin	Signal Name
1	DRV_ACT#
2	No connect

1.12.2.2 PC/PCI Connector

The PC/PCI connector is a 2 x 3-pin connector (J6D1) that may be used by some PCI add-in boards that require ISA DMA functionality. The most common example of this would be a PCI audio card. The ISA DMA functionality is required for true Sound Blaster† compatibility.

Table 26. PC/PCI Connector (J6D1)

Pin	Signal Name
1	P_PCIGNTA#
2	Ground
3	No connect
4	P_PCIREQA#
5	Ground
6	SER_IRQ

1.12.2.3 Power Supply Connector

When used with an ATX-compliant power supply that supports remote power on/off, the motherboard can turn off the system power through software control. See Section 6.2 for information about the ATX specification.

To enable soft-off control in software, advanced power management (APM) must be enabled in the Setup program and in the operating system. When the system BIOS receives the correct APM command from the operating system, the BIOS turns off power to the computer.

With soft-off enabled, if power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off).

Table 27. Power Supply Connector (J7L1)

Pin	Signal Name
1	+3.3 V
2	+3.3 V
3	Ground
4	+5 V
5	Ground
6	+5 V
7	Ground
8	PWRGD (Power Good)
9	+5 VSB
10	+12 V
11	+3.3 V
12	-12 V
13	Ground
14	PS-ON# (power supply remote on/off control)
15	Ground
16	Ground
17	Ground
18	-5 V
19	+5 V
20	+5 V

⟹ NOTE

The pin numbers in Table 27 relate to the pins of the ATX power supply connector itself, and not the pin numbers that are silk-screened on the motherboard.

1.12.3 Front Panel Connectors

The front panel connector includes connections for the following:

- Offboard speaker
- Reset switch
- Sleep/Power/Message Waiting LED
- Hard drive activity LED
- Infrared port
- Sleep/Resume switch
- Power switch

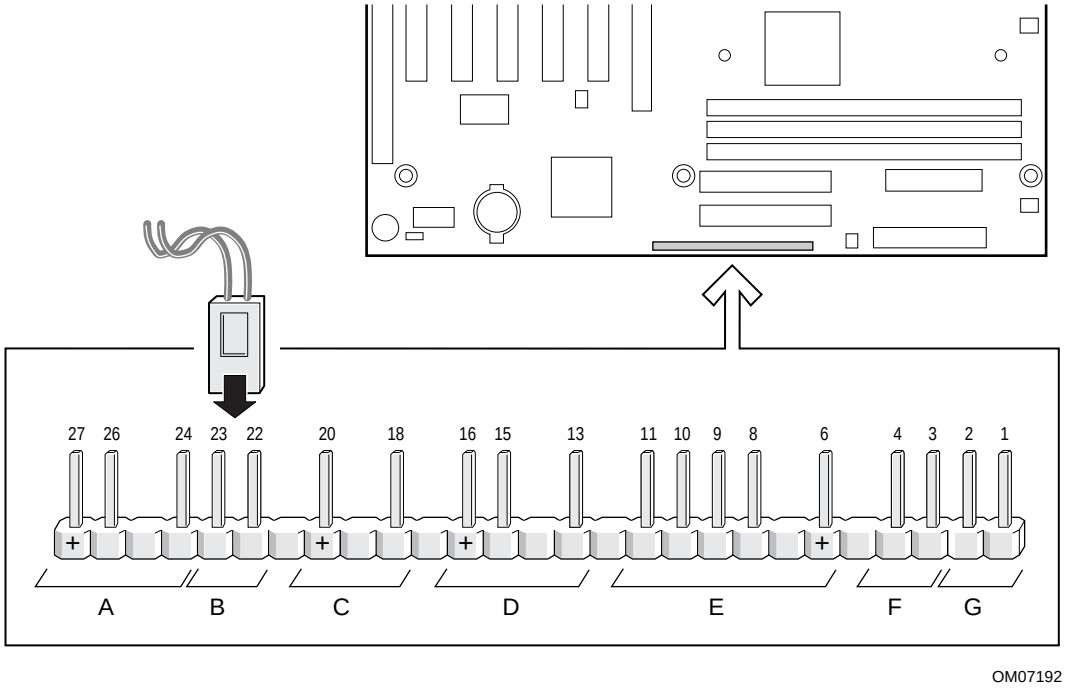


Figure 6. Front Panel I/O Connectors

Table 28. Front Panel I/O Connectors (J8G2)

Connector	Pin	Signal Name	Connector	Pin	Signal Name
A. Offboard Speaker (SPEAKER)	27	SPKR		13	HD_PWR +5 V (5 V, 15 mA max.)
	26	SPKR	none	12	Key
	25	Key	E. Infrared (IrDA) Port (INFRARED)	11	+5 V
	24	Ground		10	IR_TX
B. Reset Switch (RESET)	23	FP_RESET#		9	Ground
	22	Ground		8	IR_RX
none	21	Key		7	Key
C. Sleep/Power/Msg. Waiting LED (PWR/LED)	20	PWR_LED1 (green)		6	+5 V
	19	Key	none	5	Key
	18	PWR_LED0 (yellow)	F. Sleep/Resume Sw. (SLEEP)	4	Ground
none	17	Key		3	SLEEP_REQ#
D. Hard Drive Activity LED (HD LED)	16	HD_PWR (5 V, 15 mA max.)	G. Power Switch (PWR ON)	2	Ground
	15	HD Active#		1	SW_ON#
	14	Key			

1.12.3.1 Offboard Speaker Connector

An offboard speaker can be connected to the motherboard at the front panel connector. The speaker (onboard or offboard) provides error beep code information during the POST in the event that the computer cannot use the video interface. The speaker is not connected to the audio subsystem and does not receive output from the audio subsystem.

1.12.3.2 Reset Switch Connector

This connector can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the motherboard resets and runs the POST.

1.12.3.3 Sleep/Power/Message Waiting LED Connector

This header can be connected to a single- or dual-colored LED. Table 29 shows the possible states for a single-colored LED. Table 30 shows the possible states for a dual-colored LED.

Table 29. States for a Single-colored Power LED

LED State	Description
Off	Power off
Steady Green	Running
Blinking Green	Running/message waiting

Table 30. States for a Dual-colored Power LED

LED State	Description
Off	Power off
Steady Green	Running
Blinking Green	Running/message waiting
Steady Yellow	Sleeping
Blinking Yellow	Sleeping/message waiting

NOTE

To utilize the message waiting function, a message-capturing software application must be invoked.

1.12.3.4 Hard Drive LED Activity Connector

This connector can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. For the LED to function properly, an IDE drive must be connected to the onboard hard drive controller. This LED will also show activity for devices connected to the SCSI hard drive LED connector. See Section 1.12.2.1 for information about the SCSI LED connector.

1.12.3.5 Infrared Port Connector

Serial Port B can be configured to support an IrDA module connected to this 6-pin connector. After the IrDA interface is configured, files can be transferred to or from portable devices such as laptops, PDAs, and printers using application software.

1.12.3.6 Sleep/Resume Switch Connector

When APM is enabled in the system BIOS, and the operating system's APM driver is loaded, the system can enter sleep (standby) mode in one of the following ways:

- Optional front panel sleep/resume button
- Prolonged system inactivity using the BIOS inactivity timer feature (see Section 4.5)

The 2-pin connector located on the front panel I/O connector supports a front panel sleep/resume switch, which must be a momentary SPST type that is normally open.

Closing the sleep/resume switch sends a System Management Interrupt (SMI) to the processor, which immediately goes into SMM. While the computer is in sleep mode, it is fully capable of responding to and servicing external interrupts (such as an incoming fax) even though the monitor turns on only if a keyboard or mouse interrupt occurs. To reactivate or resume system operation, the sleep/resume switch must be pressed again, or the keyboard or mouse must be used.

1.12.3.7 Power Switch Connector

This connector can be connected to a front panel power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the motherboard.) At least two seconds must pass before the power supply will recognize another on/off signal.

1.12.4 Add-in Board Expansion Connectors

There are four PCI slots and one shared slot (for a PCI or ISA card) on the motherboard. The PCI bus supports up to five bus masters through the five PCI connectors (see Section 6.2 for information about compliance with the PCI specification).

Table 31. PCI Bus Connectors

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	Ground (TRST#)*	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	Ground (TCK)*	A33	+3.3 V	B33	C/BE2#
A3	+5 V (TMS)*	B3	Ground	A34	FRAME#	B34	Ground
A4	+5 V (TDI)*	B4	no connect (TDO)*	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#
A9	Reserved	B9	no connect (PRSNT1#)*	A40	+5 V (SDONE)*	B40	PERR#
A10	+5 V (I/O)	B10	Reserved	A41	+5 V (SBO#)*	B41	+3.3 V
A11	Reserved	B11	no connect (PRSNT2#)*	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	+3.3 V aux	B14	Reserved	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V (I/O)	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	PME#	B19	+5 V (I/O)	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01
A28	AD22	B28	Ground	A59	+5 V (I/O)	B59	+5 V (I/O)
A29	AD20	B29	AD21	A60	REQ64C#	B60	ACK64C#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

* These signals (in parentheses) are optional in the PCI specification and are not currently implemented.

Table 32. ISA Bus Connectors

Pin	Signal Name	Pin	Signal Name
B1	Ground	A1	IOCHK# (IOCHCK#)
B2	RESET (RESDRV)	A2	SD7
B3	+5 V	A3	SD6
B4	IRQ9	A4	SD5
B5	-5 V	A5	SD4
B6	DRQ2	A6	SD3
B7	-12 V	A7	SD2
B8	SRDY# (NOWS#)	A8	SD1
B9	+12 V	A9	SD0
B10	Ground	A10	IOCHRDY (CHRDY)
B11	SMEMW# (SMWTC#)	A11	AEN
B12	SMEMR# (SMRDC#)	A12	SA19
B13	IOW# (IOWC#)	A13	SA18
B14	IOR# (IORC#)	A14	SA17
B15	DACK3#	A15	SA16
B16	DRQ3	A16	SA15
B17	DACK1#	A17	SA14
B18	DRQ1	A18	SA13
B19	REFRESH#	A19	SA12
B20	BCLK	A20	SA11
B21	IRQ7	A21	SA10
B22	IRQ6	A22	SA9
B23	IRQ5	A23	SA8
B24	IRQ4	A24	SA7
B25	IRQ3	A25	SA6
B26	DACK2#	A26	SA5
B27	TC	A27	SA4
B28	BALE	A28	SA3
B29	+5 V	A29	SA2
B30	OSC	A30	SA1
B31	Ground	A31	SA0
Key		Key	
D1	MEMCS16# (M16#)	C1	SBHE#
D2	IOCS16# (IO16#)	C2	LA23
D3	IRQ10	C3	LA22

Note: Items in parentheses are alternate versions of signal names.

continued

Table 32. ISA Bus Connectors (continued)

Pin	Signal Name	Pin	Signal Name
D4	IRQ11	C4	LA21
D5	IRQ12	C5	LA20
D6	IRQ15	C6	LA19
D7	IRQ14	C7	LA18
D8	DACK0#	C8	LA17
D9	DRQ0	C9	MEMR# (MRDC#)
D10	DACK5#	C10	MEMW# (MWTC#)
D11	DRQ5	C11	SD8
D12	DACK6#	C12	SD9
D13	DRQ6	C13	SD10
D14	DACK7#	C14	SD11
D15	DRQ7	C15	SD12
D16	+5 V	C16	SD13
D17	Master16# (MASTER#)	C17	SD14
D18	Ground	C18	SD15

Note: Items in parentheses are alternate versions of signal names.

1.13 Jumper Settings

The motherboard has a single jumper block at location J8A1. The 3 pin jumper enables all motherboard configuration to be done in Setup. Figure 7 shows the location of the configuration jumper block. Table 33 describes the jumper settings for normal, configure, and recovery modes.

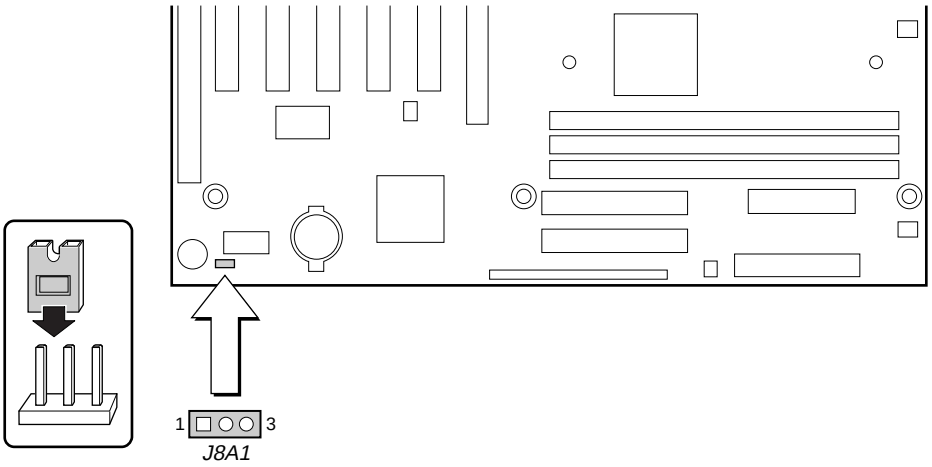


Figure 7. Location of the Configuration Jumper Block

Table 33. Configuration Jumper Settings

Function	Jumper J8A1	Configuration
Normal	1-2	The BIOS uses current configuration information and passwords for booting.
Configure	2-3	After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	none	The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

⚠ CAUTION

Do not move the jumper with the power on. Always turn off the power and unplug the power cord from the computer before changing the jumper.

NOTE

There is no separate jumper block for configuring the processor speed or bus frequency. The processor speed can be changed in the Setup program by using configure mode.

1.14 Mechanical Considerations

1.14.1 Form Factor

The motherboard is designed to fit into a standard ATX form-factor chassis. The outer dimensions are 12 x 7.75 inches. Figure 8 shows that the mechanical form factor, the I/O connector locations, and the mounting hole locations are in compliance with the ATX specification (see Section 6.2).

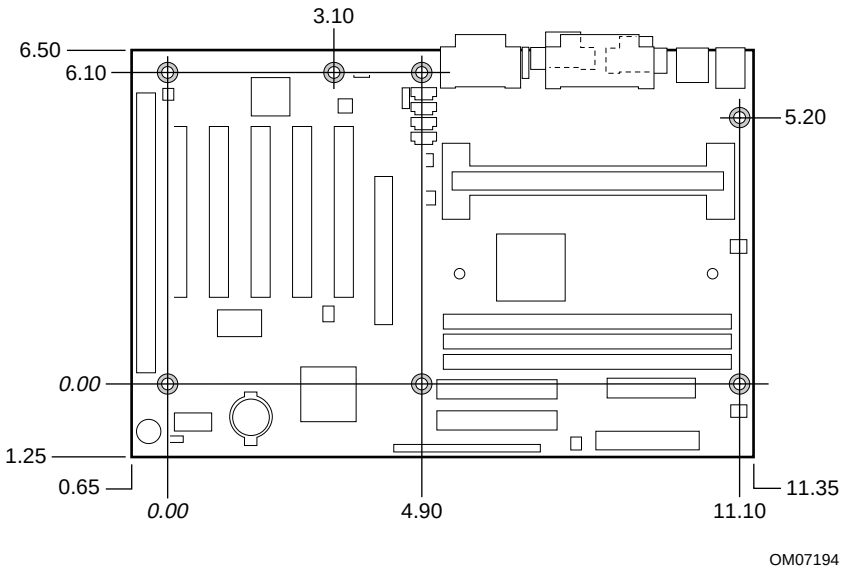


Figure 8. Motherboard Dimensions

1.14.2 I/O Shield

The back panel I/O shield for the motherboard must meet specific dimension and material requirements. Systems based on this motherboard need the back panel I/O shield to pass certification testing. Figure 9 shows the critical dimensions of the chassis-dependent I/O shield. Figure 10 shows the critical dimensions of the chassis-independent I/O shield. Figure 11 shows the critical dimensions of a chassis-independent I/O shield that accommodates the optional diagnostic LEDs (see Section1.10). Dimensions are given in inches. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification. See Section 6.2 for information about the ATX specification.

NOTE

An I/O shield specifically designed for the Intel® ATX chassis is available from Intel.

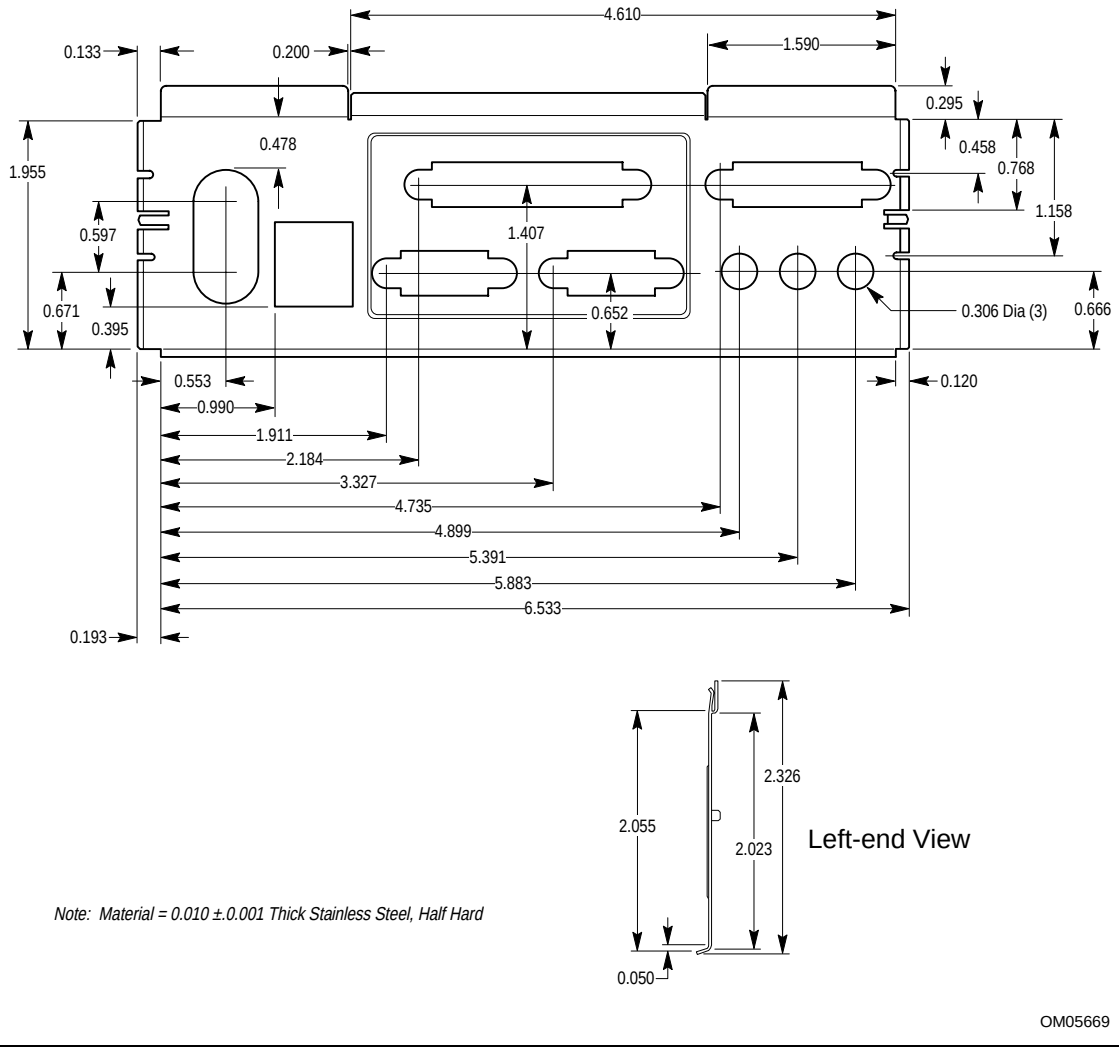


Figure 9. Back Panel I/O Shield Dimensions (ATX Chassis Dependent)

NOTE

A chassis-independent I/O shield designed to be compliant with the ATX chassis specification 2.01 is available from Intel.

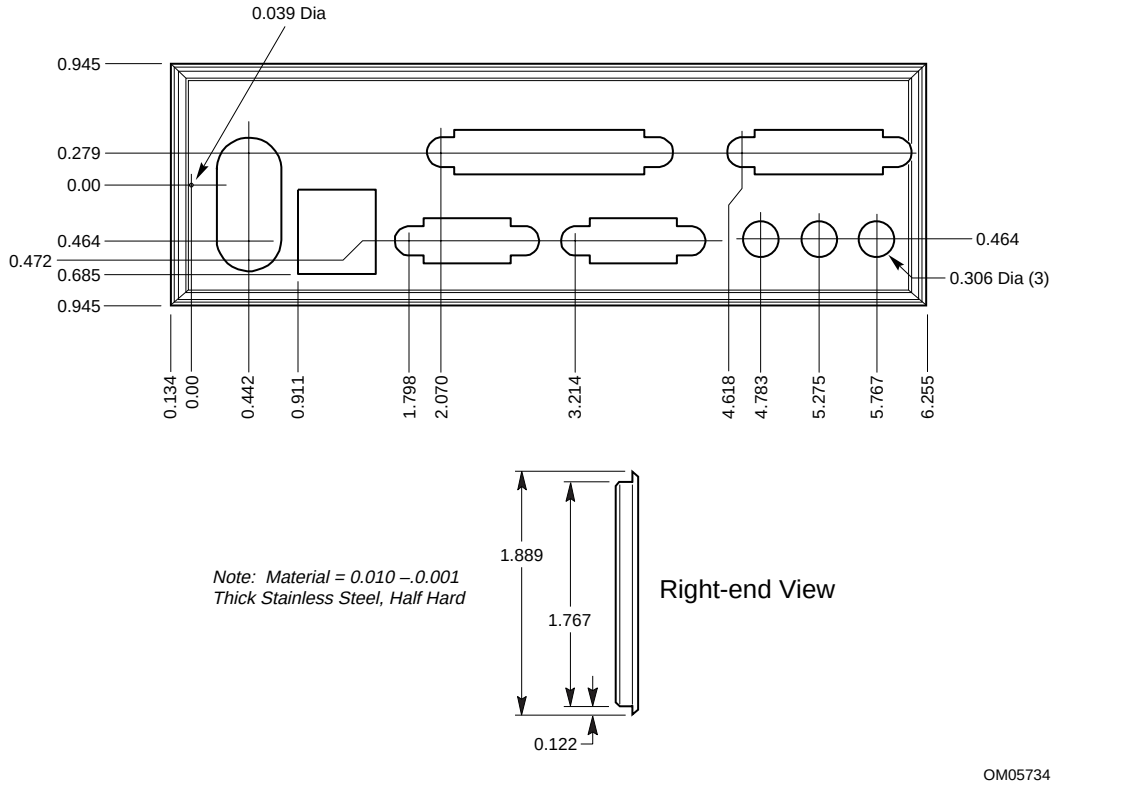


Figure 10. Back Panel I/O Shield Dimensions (ATX Chassis Independent)

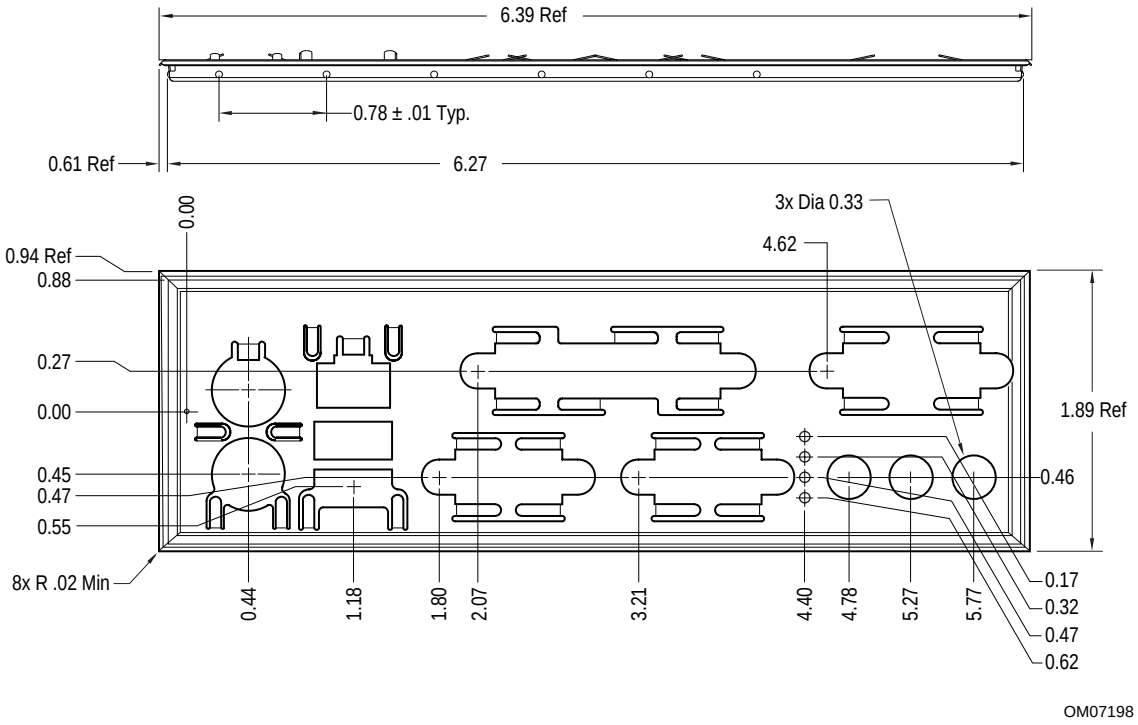


Figure 11. Back Panel I/O Shield for Motherboards with Extended Diagnostics Option (ATX Chassis Independent)

1.15 Electrical Considerations

Table 34 lists the power usage for a computer that contains a motherboard with a Pentium II processor 450 MHz, 48 MB SDRAM, 3.5-inch diskette drive, 4.3 GB UDMA IDE hard drive, 24X IDE CD-ROM drive, and an AGP graphics card. This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows 95 and Windows 98 desktop mode were measured at 65K colors and 75 Hz refresh rate. AC watts are measured with a typical ATX supply, nominal input voltage and frequency, with a true RMS wattmeter at the line input.

Table 34. Power Usage

Mode	AC Watts (out of 110 VAC wall outlet)	DC Amps (at):			
		3.3 V	5 V	+12 V	-12 V
DOS prompt, APM disabled	47 W	1.98 A	3.42 A	350 mA	10 mA
Windows 95 desktop, APM disabled	45 W	1.8 A	3.3 A	210 mA	14 mA
Windows 95 desktop, APM enabled, in SMM	30 W	1.85 A	1.3 A	210 mA	16 mA
Windows 98 desktop, ACPI disabled	34 W	1.7 A	1.6 A	210 mA	16 mA
Windows 98, ACPI S1 state	29 W	1.7 A	1.2 A	210 mA	16 mA

1.15.1 Power Supply Considerations

System integrators should refer to the power usage values listed in Table 34 when selecting a power supply for use with this motherboard. The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification (see Section 6.2).

- The potential relation between 3.3VDC and +5VDC power rails (Section 4.2 of the ATX form factor specification)
- The current capability of the +5VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

1.16 Thermal Considerations

Table 35 lists maximum component case temperatures for motherboard components that could be sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the motherboard.

CAUTION

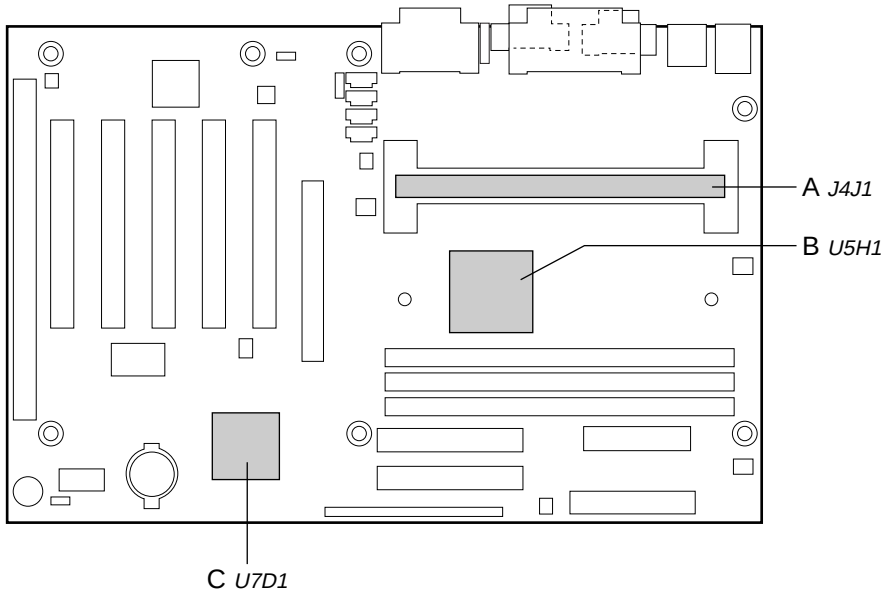
An ambient temperature that exceeds the board's maximum operating temperature by 5 °C to 10 °C might cause components to exceed their maximum case temperature. For information about the maximum operating temperature, see the environmental specifications in Section 1.17.

Table 35. Thermal Considerations for Components

Component	Maximum Case Temperature			Motherboard Location
	SECC		SECC2	
Pentium II processor	233 MHz	75 °C (thermal plate)		J4J1 (242-contact slot connector)
	266 MHz	75 °C (thermal plate)		
	300 MHz	72 °C (thermal plate)		
	333 MHz	65 °C (thermal plate)		
	350 MHz	75 °C (thermal plate)	90 °C (thermal junction)*	
	400 MHz	75 °C (thermal plate)	90 °C (thermal junction)*	
	450 MHz	75 °C (thermal plate)	90 °C (thermal junction)*	
	SEPP			
Celeron processor	266 MHz	85 °C (thermal case)		
	300 MHz	85 °C (thermal case)		
	300A MHz	85 °C (thermal case)		
	333 MHz	85 °C (thermal case)		
	366 MHz	85 °C (thermal case)		
	400 MHz	85 °C (thermal case)		
Intel 82443BX (PAC)	105 °C			U5H1
Intel 82371EB (PIIX4E)	85 °C			U7D1

* The SECC2 does not implement a thermal plate. In this case the maximum operating temperature is based on the thermal junction temperature.

Figure 12 shows motherboard components that may be sensitive to thermal changes.



A Processor (in 242-contact slot connector)
B Intel 82443BX
C Intel 82371EB

Figure 12. Thermally-Sensitive Components

1.17 Environmental Specifications

Table 36. Environmental Specifications

Parameter	Specification		
Temperature			
Nonoperating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	50 g trapezoidal waveform		
	Velocity change of 170 inches/sec		
Packaged	Half sine 2 millisecond		
	Product Weight (lbs)	**Free Fall (inches)**	**Velocity Change (inches/sec)**
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz: 0.01 g^2 Hz sloping up to 0.02 g^2 Hz		
	20 Hz to 500 Hz: 0.02 g^2 Hz (flat)		
Packaged	10 Hz to 40 Hz: 0.015 g^2 Hz (flat)		
	40 Hz to 500 Hz: 0.015 g^2 Hz sloping down to 0.00015 g^2 Hz		
Humidity			
Non-operating	non-condensing		
Operating	non-condensing		

1.18 Reliability

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is for estimating repair rates and spare parts requirements.

MTBF data is calculated from predicted data @ 55 °C.

The MTBF prediction for the motherboard is 188,374 hours.

1.19 Regulatory Compliance

This motherboard complies with the following safety and EMC regulations when correctly installed in a compatible host system.

Table 37. Safety Regulations

Regulation	Title
UL 1950/CSA950, 3rd edition, Dated 07-28-95	Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
EN 60950, 2nd Edition, 1992 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Community)
IEC 950, 2nd edition, 1991 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)
EMKO-TSE (74-SEC) 207/94	Summary of Nordic deviations to EN 60950. (Norway, Sweden, Denmark, and Finland)

Table 38. EMC Regulations

Regulation	Title
FCC Class B	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, pertaining to unintentional radiators. (USA)
CISPR 22, 2nd Edition, 1993 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)
VCCI Class B (ITE)	Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)
EN55022 (1994) (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)
EN50082-1 (1992)	Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3, and -4. (Europe)
ICES-003 (1997)	Interference-Causing Equipment Standard, Digital Apparatus, Class B (Including CRC c.1374). (Canada)

This printed circuit assembly has the following product certification markings:

- UL Joint Recognition Mark: Consists of small c followed by a stylized backward UR and followed by a small US (Component side)
- Manufacturer's recognition mark: Consists of a unique UL recognized manufacturer's logo, along with a flammability rating (94V-0) (Solder side)
- UL File Number for motherboards: E139761 (Component side)
- PB Part Number: Intel bare circuit board part number 723424-001 (Solder side)
- Battery "+ Side Up" marking: located on the component side of the board in close proximity to the battery holder
- FCC Logo/Declaration: (Solder side)
- CE Mark: (Component side) The CE mark should also be on the shipping container
- ACA Mark (C-Tick): Consists of a stylized letter c with a tick mark and the number N-232. This mark is not required on motherboards. Boxed versions must include this mark on the container only

2 Motherboard Resources

2.1 Memory Map

Table 39. Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 786432 K	100000 - 2EE00000	767 MB	Extended memory
928 K - 1024 K	E8000 - FFFFF	96 KB	System BIOS
896 K - 928 K	E0000 - E7FFF	32 KB	System BIOS (Available as UMB)
800 K - 896 K	C8000 - DFFFF	96 KB	Available high DOS memory (open to ISA and PCI buses)
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
0 K - 640 K	00000 - 9FFFF	640 KB	Conventional memory

2.2 DMA Channels

Table 40. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8 or 16 bits	Audio
1	8 or 16 bits	Audio/parallel port
2	8 or 16 bits	Diskette drive
3	8 or 16 bits	Parallel port (for ECP)/audio
4		Reserved - cascade channel
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

2.3 I/O Map

Table 41. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	DMA controller 1
0020 - 0021	2 bytes	Interrupt controller 1
002E - 002F	2 bytes	Super I/O controller configuration registers
0040 - 0043	4 bytes	Counter/Timer 1
0048 - 004B	4 bytes	Counter/Timer 2
0060	1 byte	Keyboard controller
0061	1 byte	NMI, speaker control
0064	1 byte	Keyboard controller
0070 - 0071	2 bytes	Real time clock controller
0080 - 008F	16 bytes	DMA page registers
00A0 - 00A1	2 bytes	Interrupt controller 2
00B2 - 00B3	2 bytes	APM control
00C0 - 00DE	31 bytes	DMA controller 2
00F0 - 00FF	16 bytes	Numeric processor
0120 - 0127	8 bytes	Audio controller
0170 - 0177	8 bytes	Secondary IDE controller
01F0 - 01F7	8 bytes	Primary IDE controller
0201, or (Note 1)	1 byte	Audio / game port / joy stick
0202, or		
0204, or		
0205		
0220 - 022F	16 bytes	Audio (Sound Blaster compatible)
0228 - 022F	8 bytes	LPT3
0240 - 024F	16 bytes	Audio (Sound Blaster compatible)
0260 - 026F	16 bytes	Audio (Sound Blaster compatible)
0274 - 0277	4 bytes	I/O read data port for ISA Plug and Play enumerator
0278 - 027F	8 bytes	LPT2
0280 - 028F	16 bytes	Audio (Sound Blaster compatible)
02E8 - 02EF	8 bytes	COM4/Video (8514A)
02F8 - 02FF	8 bytes	COM2
0300 - 0301, or (Note 1)	2 bytes	MPU-401 (MIDI)
0330 - 0331, or		
0332 - 0333, or		
0334 - 0335		
0376 - 0377	2 bytes	Secondary IDE controller
0378 - 037F	8 bytes	LPT1
0388 - 038B	4 bytes	AdLib† (FM synthesizer)
0398 - 039B, or (Note 1)		
03A0 - 03A3, or		
03A8 - 03AB, or		
03B0 - 03BB	12 bytes	Video (monochrome)
03C0 - 03DF	32 bytes	Video (VGA)

continued

Table 41. I/O Map (continued)

Address (hex)	Size	Description
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5, 03F7	7 bytes	Diskette controller
03F6	1 byte	Primary IDE controller
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
0530 - 0537	8 bytes	Windows Sound System
LPT*n* + 400h	8 bytes	ECP port, LPT*n* base address + 400h
0CF8 - 0CFF (Note 2)	8 bytes	PCI configuration registers
0CF9 (Note 3)	1 byte	Turbo and reset control register

Notes:

1. These are the four possible starting addresses for this device.
2. DWORD access only.
3. Byte access only.

2.4 PCI Configuration Space Map

Table 42. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Intel 82443BX (PAC)
00	01	00	Intel 82443BX PCI-to-PCI bridge (for AGP)
00	07	00	Intel 82371EB (PIIX4E) PCI/ISA bridge
00	07	01	Intel 82371EB (PIIX4E) IDE bus master
00	07	02	Intel 82371EB (PIIX4E) USB
00	07	03	Intel 82371EB (PIIX4E) power management
00	0C	00	PCI audio (Yamaha YMF724 audio controller)
00	0D	00	PCI bus connector 1 (J4D2)
00	0E	00	PCI bus connector 2 (J4D1)
00	0F	00	PCI bus connector 3 (J4C1)
00	10	00	PCI bus connector 4 (J4B1)
00	11	00	PCI bus connector 5 (J4A1)
01	00	00	AGP connector (J4E1)

2.5 Interrupts

Table 43. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard controller
2	Reserved, cascade interrupt from slave PIC
3	COM2*
4	COM1*
5	LPT2 (Plug and Play option)/audio/user available
6	Diskette drive controller
7	LPT1*
8	Real time clock
9	Reserved
10	USB/user available
11	Windows Sound System*/user available
12	PS/2 mouse port (if present, else user available)
13	Reserved, numeric processor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

* Default, but can be changed to another IRQ

2.6 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI expansion slots and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The PIIX4E PCI-to-ISA bridge has four programmable interrupt request (PIRQ) input signals. Any PCI interrupt source (either onboard or from a PCI add-in card) connects to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are mechanically tied together on the motherboard and therefore share the same interrupt. Table 44 lists the PIRQ signals and shows how the signals are connected to the onboard PCI interrupt sources.

Table 44. PCI Interrupt Routing Map

PIIX4E PIRQ Signal	First PCI Bus Connector (J4D2)	Second PCI Bus Connector (J4D1)	Third PCI Bus Connector (J4C1)	Fourth PCI Bus Connector (J4B1)	Fifth PCI Bus Connector (J4A1)	PCI Audio	AGP Slot: J4E1	USB
PIRQA	INTA	INTD	INTC	INTB	INTC		INTA	
PIRQB	INTB	INTA	INTD	INTC	INTD		INTB	
PIRQC	INTC	INTB	INTA	INTD	INTA			
PIRQD	INTD	INTC	INTB	INTA	INTB	INTA		INTA

For example, assume an add-in card has one interrupt (group INTA) and is installed in the fourth PCI connector. In this connector, an interrupt source from group INTA connects to the PIRQD signal, which is already connected to the USB and audio sources. The add-in card shares an interrupt with these onboard interrupt sources.

NOTE

The PIIX4E can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 7, 9, 11, 14, 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

3 Overview of BIOS Features

The motherboard uses an Intel/Phoenix BIOS, which is stored in flash memory and can be upgraded using a disk-based program. In addition to the BIOS, the flash memory contains the Setup program, POST, APM, ACPI, the PCI auto-configuration utility, and Windows 95 and Windows 98-ready Plug and Play.

This motherboard supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOS is identified as 4S4EB3X0.86A.

3.1 BIOS Flash Memory Organization

The Intel® E28F004S5 is a high performance 4 Mbit (512 KB) symmetrical flash memory device. Internally, the device is grouped into eight 64-KB blocks that are individually erasable, lockable, and unlockable. Figure 13 shows the organization of the flash memory.

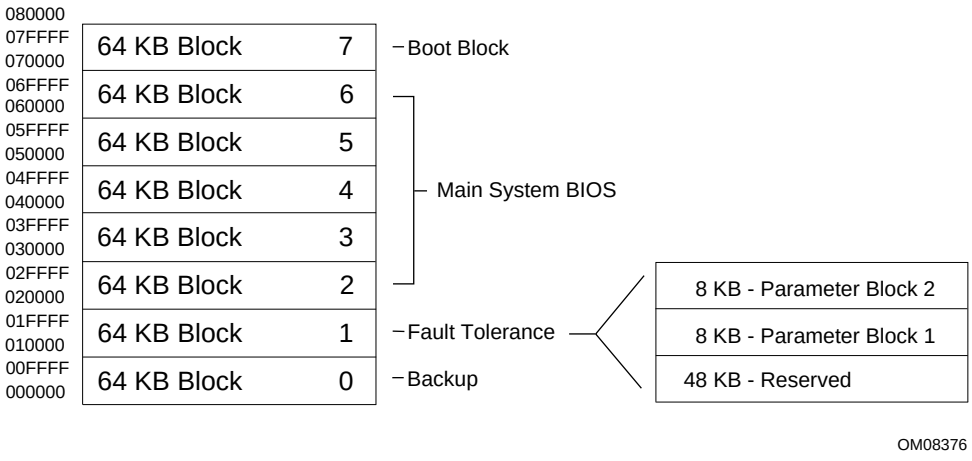


Figure 13. Memory Map of the Flash Memory Device

Symmetrical flash memory allows both the boot and the fault tolerance blocks to increase in size from 16 KB to 64 KB. This increase allows the addition of features such as dynamic memory detection, LS-120 recovery code, and extended security features.

The last two 8 KB blocks of the fault tolerance area are the parameter blocks. These blocks contain data such as BIOS updates, vital product data (VPD), logo, System Management BIOS (SMBIOS) interface, and extended system configuration data (ESCD) information. The backup block contains a copy of the fault tolerance block.

3.2 Resource Configuration

3.2.1 Plug and Play: PCI Autoconfiguration

The BIOS can automatically configure PCI devices and Plug and Play devices. PCI devices may be onboard or add-in cards. Plug and Play devices are ISA devices built to meet the Plug and Play specification. Autoconfiguration lets a user insert or remove PCI or Plug and Play cards without having to configure the system. When a user turns on the system after adding a PCI or Plug and Play card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup (see Section 4.3.7) are considered to be available for use by the add-in card.

PCI interrupts are distributed to available ISA interrupts that have not been assigned to an ISA card or to system resources. The assignment of PCI interrupts to ISA IRQs is nondeterministic. PCI devices can share an interrupt, but an ISA device cannot share an interrupt allocated to PCI or to another ISA device. Autoconfiguration information is stored in ESCD format. For information about the versions of PCI and Plug and Play supported by this BIOS, see Section 6.2.

3.2.2 ISA Plug and Play

If Plug & Play OS (see Section 4.3) is selected in Setup, the BIOS autoconfigures only ISA Plug and Play cards that are required for booting (IPL devices). If Plug and Play operating system is not selected in Setup, the BIOS autoconfigures all Plug and Play ISA cards.

3.2.3 PCI IDE Support

If Auto (see Section 4.3.3) is selected in Setup, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface recognizes any ATAPI devices, including CD-ROM drives, tape drives and Ultra DMA drives and supports the transfer modes listed in Table 56 (see Section 6.2 for the supported version of ATAPI). Add-in ISA IDE controllers are not supported. The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in Setup.

⟹ NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device.

3.3 System Management BIOS (SMBIOS)

System Management BIOS (SMBIOS) is an interface for managing computers in an enterprise environment. The main component of SMBIOS is the management information format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as Intel® LANDesk® Client Manager to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT, require an additional interface for obtaining SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, a SMBIOS service-level application running on a non-Plug and Play OS can access the SMBIOS BIOS information.

See Section 6.2 for SMBIOS specification information.

3.4 Power Management

The BIOS supports both APM and ACPI. If the board is used with an ACPI-aware operating system, the BIOS provides ACPI support. Otherwise, it defaults to APM support.

3.4.1 Advanced Power Management (APM)

See Section 6.2 for the version of the APM specification that is supported. The energy saving standby mode can be initiated in the following ways:

- Time-out period specified in Setup
- Suspend/resume switch connected to the front panel sleep connector
- From the operating system, such as the Suspend menu item in Windows 95

In standby mode, the motherboard can reduce power consumption by spinning down hard drives, and reducing power to or turning off VESA† DPMS-compliant monitors. Power-management mode can be enabled or disabled in Setup (see Section 4.5).

While in standby mode, the system retains the ability to respond to external interrupts and service requests, such as incoming faxes or network messages. Any keyboard or mouse activity brings the system out of standby mode and immediately restores power to the monitor.

The BIOS enables APM by default; but the operating system must support an APM driver for the power-management features to work. For example, Windows 95 supports the power-management features upon detecting that APM is enabled in the BIOS.

3.4.2 Advanced Configuration and Power Interface (ACPI)

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. ACPI requires an ACPI-aware operating system. ACPI features include:

- Plug and Play (including bus and device enumeration) and APM functionality normally contained in the BIOS
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 30-watt system operation in the Power On Suspend sleeping state, and less than 5-watt system operation in the Suspend to Disk sleeping state
- A Soft-off feature that enables the operating system to power off the computer
- Support for multiple wake up events (see Table 47)
- Support for a front panel power and sleep mode switch. Table 45 describes the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system

Table 45. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off	Less than four seconds	Power on
On	Less than four seconds	Soft off/Suspend
On	More than four seconds	Fail safe power off
Sleep	Less than four seconds	Wake up

3.4.2.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 46 lists the power states supported by the motherboard along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 46. Power States and Targeted System Power

Global States	Sleeping States	CPU States	Device States	Targeted System Power *
G0 - working state	N/A	C0 – working	D0 - working state	Full power > 60 W
G1 - sleeping state	S1 - CPU stopped	C1 - stop grant	D1, D2, D3- device specification specific.	5 W < power < 30 W
G1 - sleeping state***	S3 - Suspend to RAM. Context saved to RAM.	No power	D3 - no power except for wake up logic.	Power < 5 W **
G1 - sleeping state	S4BIOS - suspend to disk. Context saved to disk.	No power	D3 - no power except for wake up logic.	Power < 5 W **
G2/S5	S5 - Soft off. Context not saved. Cold boot is required.	No power	D3 - no power except for wake up logic.	Power < 5 W **
G3 - mechanical off. AC power is disconnected from the computer.	No power to the system.	No power	D3 - no power for wake up logic, except when provided by battery or external source.	No power to the system so that service can be performed.

* Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.

** Assumes limited number of wake up devices.

*** Suspend to RAM option.

3.4.2.2 Wake Up Devices and Events

The table below describes which devices or specific events can wake the computer from specific states. Sleeping states S4BIOS and S5 are the same for the wake up events.

Table 47. Wake Up Devices and Events

These devices/events can wake up the computer…	…from this state
Power switch	S1, S3*, S4BIOS, S5
RTC alarm	S1, S3*, S4BIOS, S5
LAN	S1, S3*, S4BIOS, S5
Modem	S1, S3*, S4BIOS, S5
Thermal event	S1, S3*, S4BIOS
IR command	S1
USB	S1
PS/2 keyboard	S1
PS/2 mouse	S1

* Suspend to RAM option

3.4.2.3 Plug and Play

In addition to power management, ACPI provides controls and information so that the operating system can facilitate Plug and Play device enumeration and configuration. ACPI is used only to enumerate and configure motherboard devices that do not have other hardware standards for enumeration and configuration. PCI devices on the motherboard, for example, are not enumerated by ACPI.

3.5 BIOS Upgrades

A new version of the BIOS can be upgraded from a diskette using the Intel® Flash Memory Update Utility that is available from Intel. This utility supports the following BIOS maintenance functions:

- Update the flash BIOS from a file on a diskette
- Change the language section of the BIOS
- Verify that the upgrade BIOS matches the target system to prevent accidentally installing an incompatible BIOS

BIOS upgrades and the Intel Flash Memory Update Utility are available from Intel through the Intel World Wide Web site. See Section 6.1 for information about this site.

⟹ NOTE

Please review the instructions distributed with the upgrade utility before attempting a BIOS upgrade.

3.5.1 Language Support

The Setup program and help messages can be supported in 32 languages. Five languages are available: American English, German, Italian, French, and Spanish. The default language is American English, which is present unless another language is programmed into the BIOS using the flash memory update utility. See Section 3.1 for information about the BIOS update utility.

The BIOS includes extensions to support the Kanji character set and other non-ASCII character sets. Translations of other languages may become available at a later date.

3.5.2 OEM Logo or Scan Area

An 8 KB flash-memory user area is for displaying a custom OEM logo during POST. A utility is available from Intel to assist with installing a logo into the flash memory. Information about this capability is available on the Intel Support world wide web site. See Section 6.1 for more information about this site.

3.5.3 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode (see Section 1.13). When recovering the BIOS, be aware of the following:

- Because of the small amount of code available in the nonerasable boot block area, there is no video support. The procedure can only be monitored by listening to the speaker and looking at the diskette drive LED.
- The recovery process may take several minutes; larger BIOS flash memory devices require more time.
- A single beep indicates the beginning of the BIOS recovery process.
- Two beeps and the end of activity in the diskette drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery.

To create a BIOS recovery diskette, a bootable diskette must be created and the BIOS update files copied to it. BIOS upgrades and the Intel Flash Memory Upgrade Utility are available from Intel through the Intel World Wide Web site. See Section 6.1 for information about this site.

NOTE

If the computer is configured to boot from an LS-120 diskette, the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.

NOTE

BIOS recovery cannot be accomplished using non-SPD DIMMs. SPD data structure is required for the recovery process.

3.5.4 Boot Options

In the Setup program, the user can choose to boot from a diskette drive, hard drive, CD-ROM, the network, or any BIOS boot specification (BBS) compliant device. The default setting is for the diskette drive to be the primary boot device and the hard drive to be the secondary boot device. By default the third and fourth devices are disabled.

3.5.5 CD-ROM and Network Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. See Section 6.2 for information about the El Torito specification. Under the Boot menu in the Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. If the CD-ROM is selected as the boot device, it must be the first device.

The network can be selected as a boot device. This selection allows booting from a network add-in card with a remote boot ROM installed.

3.5.6 USB Legacy Support

USB legacy support enables USB keyboards and mice to be used even when no operating system USB drivers are in place. By default, USB legacy support is disabled. USB legacy support is only intended to be used in accessing BIOS Setup and installing an operating system that supports USB.

This sequence describes how USB legacy support operates in the default (disabled) mode.

1. When you power up the computer, USB legacy support is disabled.
2. POST begins.
3. USB legacy support is temporarily enabled by the BIOS. This allows you to use a USB keyboard to enter the Setup program or the maintenance mode.
4. POST completes and disables USB legacy support (unless it was set to Enabled while in Setup).
5. The operating system loads. While the operating system is loading, USB keyboards and mice are not recognized. After the operating system loads the USB drivers, the USB devices are recognized.

To install an operating system that supports USB, enable USB legacy support in BIOS Setup and follow the operating system's installation instructions. Once the operating system is installed and the USB drivers configured, USB legacy support is no longer used. USB legacy support can be left enabled in BIOS Setup if needed.

Notes on using USB legacy support:

- If USB legacy support is enabled, don't mix USB and PS/2 keyboards and mice. For example, do not use a PS/2 keyboard with a USB mouse, or a USB keyboard and a PS/2 mouse.
- Do not use USB devices with an operating system that does not support USB. USB legacy is not intended to support the use of USB devices in a non USB operating system.
- USB legacy support is for keyboards and mice only. Hubs and other USB devices are not supported.

3.5.7 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the Setup program. This is supervisor mode.
- The user password gives restricted access to view and change Setup options in the Setup program. This is user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 48 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 48. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options *	Can change all options *	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

* If no password is set, any user can change all Setup options.

See Section 4.4 for information about setting user and supervisor passwords.

4 BIOS Setup Program

The Setup program is for viewing and changing the BIOS settings for a computer. Setup is accessed by pressing the <F2> key after the POST memory test begins and before the operating system boot begins.

Table 49 shows the menus available from the menu bar at the top of the Setup screen.

Table 49. Setup Menu Bar

Setup Menu Screen	Description
Maintenance	Specifies the processor speed and clears the Setup passwords. This menu is only available in configure mode. Refer to Section 1.13 for information about configure mode.
Main	Allocates resources for hardware components.
Advanced	Specifies advanced features available through the chipset.
Security	Specifies passwords and security features.
Power	Specifies power management features.
Boot	Specifies boot options and power supply controls.
Exit	Saves or discards changes to the Setup program options.

Table 50 shows the function keys available for menu screens.

Table 50. Setup Function Keys

Setup Key	Description
<F1> or <Alt-H>	Brings up a help screen for the current item.
<Esc>	Exits the menu.
<←> or <→>	Selects a different menu screen.
<↑> or <↓>	Moves cursor up or down.
<Home> or <End>	Moves cursor to top or bottom of the window.
<PgUp> or <PgDn>	Moves cursor to top or bottom of the window.
<F5> or <->	Selects the previous value for a field.
<F6> or <+> or <Space>	Selects the next value for a field.
<F9>	Load the default configuration values for the current menu.
<F10>	Save the current values and exit Setup.
<Enter>	Executes command or selects the submenu.

4.1 Maintenance Menu

This menu is for setting the processor speed and clearing the Setup passwords. Setup only displays this menu in configure mode. See Section 1.13 for information about setting configure mode.

Table 51. Maintenance Menu

Feature	Options	Description
Processor Speed	• 233 • 266 • 300 • 333 • 350 • 400 • 450	Specifies the processor speed in megahertz. This setup screen will only show speeds up to and including the maximum speed of the processor installed on the motherboard. • With a host bus operating at 66 MHz, the board supports processors at the following speeds: 233, 266, 300, 333, 366, and 400 MHz. • With a host bus operating at 100 MHz, the board supports processors at the following speeds: 350, 400, 450, and 500 MHz.
Clear All Passwords	No options	Clears the user and supervisor passwords.

NOTE

Processors that run at a fixed frequency will not show an entry for processor speeds.

4.2 Main Menu

This menu reports processor and memory information and is for configuring the system date and system time.

Table 52. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS.
Processor Type	No options	Displays processor type.
Processor Speed	No options	Displays processor speed.
System Memory	No options	Displays the total amount of RAM on the motherboard.
Memory Bank 0 Memory Bank 1 Memory Bank 2	No options	Displays size and type of DIMM installed in each memory bank.
Language	• **English (US) (default)** • Francais • Italiano • Deutsch • Espanol	Selects the default language used by the BIOS.

continued

Table 52. Main Menu (continued)

Feature	Options	Description
ECC Configuration	• **Non-ECC (default)** • ECC	Specifies ECC memory operation.
L2 Cache ECC Support *	• **Disabled (default)** • Enabled	*Enabled* allows error checking to occur on data accessed from L2 cache.
System Time	Hour, minute, and second	Specifies the current time.
System Date	Month, day, and year	Specifies the current date.

NOTE: This screen option will not appear when using processors that have L2 cache ECC permanently enabled.

4.3 Advanced Menu

This menu is for setting advanced features that are available through the chipset.

Table 53. Advanced Menu

Feature	Options	Description
Plug & Play O/S	• **No (default)** • Yes	Specifies if a Plug and Play operating system is being used. *No* lets the BIOS configure all devices. *Yes* lets the operating system configure Plug and Play devices. Not required with a Plug and Play operating system.
Reset Configuration Data	• **No (default)** • Yes	Clears the BIOS configuration data on the next boot.
Numlock	• **Auto (default)** • On • Off	Specifies the power on state of the Num Lock feature on the numeric keypad of the keyboard.
Peripheral Configuration	No options	Configures peripheral ports and devices. When selected, displays the Peripheral Configuration submenu.
IDE Configuration	No options	Specifies type of connected IDE device.
Floppy Options	No options	When selected, displays the Floppy Options submenu.
DMI Event Logging	No options	Configures DMI Event Logging. When selected, displays the DMI Event Logging submenu.
Video Configuration	No options	Configures video features. When selected, displays the Video Configuration submenu.
Resource Configuration	No options	Configures memory blocks and IRQs for legacy ISA devices. When selected, displays the Resource Configuration submenu.

4.3.1 Peripheral Configuration Submenu

This submenu is for the configuring the computer peripherals.

Table 54. Peripheral Configuration Submenu

Feature	Options	Description
Serial port A	• Disabled • Enabled • **Auto (default)**	Configures serial port A. *Auto* assigns the first free COM port, normally COM1, the address 3F8h and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Base I/O address	• **3F8 (default)** • 2F8 • 3E8 • 2E8	Specifies the base I/O address for serial port A.
Interrupt	• IRQ 3 • **IRQ 4 (default)**	Specifies the interrupt for serial port A.
Serial port B	• Disabled • Enabled • **Auto (default)**	Configures serial port B. *Auto* assigns the first free COM port, normally COM2, the address 2F8h and the interrupt IRQ3. An * (asterisk) displayed next to an address indicates a conflict with another device. If either serial port address is set, that address will not appear in the list of options for the other serial port. If an *ATI*† *mach32*† or an *ATI mach64*† video controller is active as an add-in card, the COM4, 2E8h address will not appear in the list of options for either serial port.
Mode	• **Normal (default)** • IrDA • ASK-IR	Specifies the mode for serial port B for normal (COM 2) or infrared applications.
Base I/O address	• 3F8 • **2F8 (default)** • 3E8 • 2E8	Specifies the base I/O address for serial port B.
Interrupt	• **IRQ 3 (default)** • IRQ 4	Specifies the interrupt for serial port B.
Parallel port	• Disabled • Enabled • **Auto (default)**	Configures the parallel port. *Auto* assigns LPT1 the address 378h and the interrupt IRQ7. An * (asterisk) displayed next to an address indicates a conflict with another device.

continued

Table 54. Peripheral Configuration Submenu (continued)

Feature	Options	Description
Mode	• Output Only • **Bi-directional (default)** • EPP • ECP	Selects the mode for the parallel port. *Output Only* operates in AT-compatible mode. *Bi-directional* operates in bi-directional PS/2-compatible mode. *EPP* is Extended Parallel Port mode, a high-speed bi-directional mode. *ECP* is Enhanced Capabilities Port mode, a high-speed bi-directional mode.
Base I/O address	• **378 (default)** • 278 • 228	Specifies the base I/O address for the parallel port.
Interrupt	• IRQ 5 • **IRQ 7 (default)**	Specifies the interrupt for the parallel port.
Audio	• Disabled • **Enabled (default)**	Enables or disables the onboard audio subsystem.
Legacy USB support	• **Disabled (default)** • Enabled	Enables or disables USB legacy support. (Refer to Section 3.5.6 for more information.)

4.3.2 IDE Configuration

Table 55. IDE Configuration

Feature	Options	Description
IDE Controller	• Disabled • Primary • Secondary • **Both (default)**	Specifies the integrated IDE controller. *Primary* enables only the Primary IDE Controller. *Secondary* enables only the Secondary IDE Controller. *Both* enables both IDE controllers.
Hard Disk Pre-Delay	• **Disabled (default)** • 3 Seconds • 6 Seconds • 9 Seconds • 12 Seconds • 15 Seconds • 21 Seconds • 30 Seconds	Specifies the hard disk drive pre-delay.
Primary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Master submenu.
Primary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Slave submenu.
Secondary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Master submenu
Secondary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Slave submenu.

4.3.3 IDE Configuration Submenus

This submenu is for configuring IDE devices, including:

- Primary IDE master
- Primary IDE slave
- Secondary IDE master
- Secondary IDE slave

Table 56. IDE Configuration Submenus

Feature	Options	Description
Type	• None • ATAPI Removable • Other ATAPI • CD-ROM • User • IDE Removable • **Auto (default)**	Specifies the IDE configuration mode for IDE devices. *Auto* automatically fills in the transfer mode values. Other options are device dependent.
Maximum Capacity	No options	Reports the maximum capacity for the hard disk.
Multi-Sector Transfers	• Disabled • 2 Sectors • 4 Sectors • 8 Sectors • 16 Sectors	Specifies number of sectors per block for transfers from the hard drive to memory. Check the hard drive's specifications for optimum setting.
LBA Mode Control	• Disabled • Enabled	Enables or disables the LBA mode control.
Transfer Mode	• Standard • Fast PIO 1 • Fast PIO 2 • Fast PIO 3 • Fast PIO 4 • FPIO 3 / DMA 1 • FPIO 4 / DMA 2	Specifies the method for moving data to/from the drive.
Ultra DMA	• Disabled • Mode 0 • Mode 1 • Mode 2	Specifies the Ultra DMA mode for the drive.

4.3.4 Floppy Options

This submenu is for configuring the diskette drive interface.

Table 57. Floppy Options Submenu

Feature	Options	Description
Floppy Disk Controller	• Disabled • **Enabled (default)** • Auto	Disables or enables the integrated diskette drive controller.
Diskette A:	• Disabled • 360 KB 5¼″ • 1.2 MB 5¼″ • 720 KB 3½″ • **1.44/1.25 MB 3½″ (default)** • 2.88 MB 3½″	Specifies the capacity and physical size of diskette drive A.
Floppy Write Protect	• **Disabled (default)** • Enabled	Disables or enables write protect for diskette drive A.

4.3.5 DMI Event Logging

This submenu is for configuring the DMI event logging features.

Table 58. DMI Event Logging Submenu

Feature	Options	Description
Event log capacity	No options	Indicates if there is space available in the event log.
Event log validity	No options	Indicates if the contents of the event log are valid.
View DMI event log	No options	Enables viewing of DMI event log.
Clear all DMI event logs	• **No (default)** • Yes	Clears the DMI event log after rebooting.
Event Logging	• Disabled • **Enabled (default)**	Enables logging of DMI events.
ECC Event Logging	• Disabled • **Enabled (default)**	Enables logging of ECC events.
Mark DMI events as read	No options	Marks all DMI events as read.

4.3.6 Video Configuration Submenu

This submenu is for configuring video features.

Table 59. Video Configuration Submenu

Feature	Options	Description
Palette Snooping	• **Disabled (default)** • Enabled	Controls the ability of a primary PCI graphics controller to share a common palette with an ISA add-in video card.
AGP Aperture Size	• **64 MB (default)** • 256 MB	Specifies the aperture size for the AGP video controller.

4.3.7 Resource Configuration Submenu

This submenu is for configuring the memory and interrupts.

Table 60. Resource Configuration Submenu

Feature	Options	Description
Memory Reservation	• C800 - CBFF **Available (default)** | Reserved • CC00- CFFF **Available (default)** | Reserved • D000 - D3FF **Available (default)** | Reserved • D400 - D7FF **Available (default)** | Reserved • D800 - DBFF **Available (default)** | Reserved • DC00 - DFFF **Available (default)** | Reserved	Reserves specific upper memory blocks for use by legacy ISA devices.
IRQ Reservation	• IRQ3 **Available (default)** | Reserved • IRQ4 **Available (default)** | Reserved • IRQ5 **Available (default)** | Reserved • IRQ7 **Available (default)** | Reserved • IRQ10 **Available (default)** | Reserved • IRQ11 **Available (default)** | Reserved	Reserves specific IRQs for use by legacy ISA devices. An * (asterisk) displayed next to an IRQ indicates an IRQ conflict.

4.4 Security Menu

This menu is for setting passwords and security features.

Table 61. Security Menu

Feature	Options	Description
User Password Is	No options	Reports if there is a user password set.
Supervisor Password Is	No options	Reports if there is a supervisor password set.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.
Clear User Password	No Options	Clears the user password.
User Setup Access	• None • View Only • Limited Access • **Full Access (default)**	Refer to Section 3.5.7 on page 73.
Unattended Start	• **Disabled (default)** • Enabled	Enables the unattended start feature. When enabled, the computer boots, but the keyboard is locked. The user must enter a password to unlock the computer or boot from a diskette.

4.5 Power Menu

This menu is for setting power management features.

Table 62. Power Menu

Feature	Options	Description
Power Management	• Disabled • **Enabled (default)**	Enables or disables the BIOS power management feature.
Inactivity Timer	• **Off (default)** • 1 Minute • 5 Minutes • 10 Minutes • 20 Minutes • 30 Minutes • 60 Minutes • 120 Minutes	Specifies the amount of time before the computer enters standby mode.
Hard Drive	• Disabled • **Enabled (default)**	Enables power management for hard disks during standby and suspend modes.
VESA Video Power Down	• Disabled • **Standby (default)** • Suspend • Sleep	Specifies power management for video during standby and suspend modes.
Fan Always On	• **No (default)** • Yes	Select *Yes* to force the fan to remain on when the system is in a power managed state.

4.6 Boot Menu

This menu is for setting the boot features and the boot sequence.

Table 63. Boot Menu

Feature	Options	Description
Boot-Time Diagnostic Screen	• **Disabled (default)** • Enabled	Displays the diagnostics screen during boot.
Quick Boot Mode	• Disabled • **Enabled (default)**	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	• **Disabled (default)** • Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
After Power Failure	• Power On • **Last State (default)** • Stay Off	Specifies the mode of operation if an AC/Power loss occurs. *Power On* restores power to the computer. *Last State* restores the previous power state before power loss occurred. *Stay Off* keeps the power off until the power button is pressed.
On Modem Ring	• Stay Off • **Power On (default)**	Specifies how the computer responds to an incoming call on an installed modem when the power is off.
On LAN	• Stay Off • **Power On (default)**	Specifies how the computer responds to a LAN wakeup event when the power is off.
On PME	• Stay Off • **Power On (default)**	Controls how the system responds to a PCI Power Management Enable wake up event.
First Boot Device Second Boot Device Third Boot Device Fourth Boot Device	• Removable devices • Hard Drive • ATAPI CD-ROM Drive • Network Boot	Specifies the boot sequence from the available devices. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each boot device in the order listed. Changing the order of the devices changes the drive lettering.
Hard Drive	No options	Lists available hard drives. When selected, displays the Hard Drive submenu.
Removable Devices	No options	Lists available removable devices. When selected, displays the Removable Devices submenu.

4.6.1 Hard Drive Submenu

This submenu is for configuring the boot sequence for hard drives.

Table 64. Hard Drive Submenu

Options	Description
Bootable Add in Card	Specifies the boot sequence for the hard drives attached to the computer. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each device in the order listed. Changing the order of the devices changes the drive lettering.

4.6.2 Removable Devices Submenu

This submenu is for configuring the boot sequence for removable devices.

Table 65. Removable Devices Submenu

Options	Description
Legacy Floppy Drives	Specifies the boot sequence for the removable devices attached to the computer. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each device in the order listed. Changing the order of the devices changes the drive lettering.

4.7 Exit Menu

This menu is for exiting the Setup program, saving changes, and loading and saving defaults.

Table 66. Exit Menu

Feature	Description
Exit Saving Changes	Exits and saves the changes in CMOS RAM.
Exit Discarding Changes	Exits without saving any changes made in Setup.
Load Setup Defaults	Loads the factory default values for all the Setup options.
Load Custom Defaults	Loads the custom defaults for Setup options.
Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

5 Error Messages and Beep Codes

5.1 BIOS Error Messages

Table 67. BIOS Error Messages

Error Message	Explanation
Diskette drive A error	Drive A is present but fails the POST diskette tests. Check that the drive is defined with the proper diskette type in Setup and that the diskette drive is installed correctly.
Extended RAM Failed at offset: *nnnn*	Extended memory not working or not configured properly at offset *nnnn*.
Failing Bits: *nnnn*	The hexadecimal number *nnnn* is a map of the bits at the RAM address (System, Extended, or Shadow memory) that failed the memory test. Each 1 in the map indicates a failed bit.
Fixed Disk 0 Failure or Fixed Disk 1 Failure or Fixed Disk Controller Failure	Fixed disk is not working or not configured properly. Check to see if fixed disk is installed properly. Run Setup be sure the fixed-disk type is correctly identified.
Incorrect Drive A type - run SETUP	Type of diskette drive for drive A not correctly identified in Setup.
Invalid NVRAM media type	Problem with NVRAM (CMOS) access.
Keyboard controller error	The keyboard controller failed test. Try replacing the keyboard.
Keyboard error	Keyboard not working.
Keyboard error nn	BIOS discovered a stuck key and displays the scan code nn for the stuck key.
Keyboard locked - Unlock key switch	Unlock the system to proceed.
Monitor type does not match CMOS - Run SETUP	Monitor type not correctly identified in Setup.
Operating system not found	Operating system cannot be located on either drive A or drive C. Enter Setup and see if fixed disk and drive A are properly identified.
Parity Check 1	Parity error found in the system bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays ????.
Parity Check 2	Parity error found in the I/O bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays ????.
Press <F1> to resume, <F2> to Setup	Displayed after any recoverable error message. Press <F1> to start the boot process or <F2> to enter Setup and change any settings.
Real time clock error	Real-time clock fails BIOS test. May require motherboard repair.

continued

Table 67. BIOS Error Messages (continued)

Error Message	Explanation
Shadow RAM Failed at offset: *nnnn*	Shadow RAM failed at offset *nnnn* of the 64 KB block at which the error was detected.
System battery is dead - Replace and run SETUP	The CMOS clock battery indicator shows the battery is dead. Replace the battery and run Setup to reconfigure the system.
System cache error - Cache disabled	RAM cache failed the BIOS test. BIOS disabled the cache.
System CMOS checksum bad - run SETUP	System CMOS RAM has been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS. Run Setup and reconfigure the system either by getting the default values and/or making your own selections.
System RAM Failed at offset: *nnnn*	System RAM failed at offset *nnnn* of the 64 KB block at which the error was detected.
System timer error	The timer test failed. Requires repair of system motherboard.

nnnn = hexadecimal number

5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires an add-in card (often called a POST card). The POST card can decode the port and display the contents on a medium such as a seven-segment display. These cards can be purchased from JDR Microdevices or other sources.

The following table provides the POST codes that can be generated by the BIOS. Some codes are repeated in the table because that code applies to more than one operation.

Table 68. Port 80h Codes

Code	Description of POST Operation
02h	Verify real mode
03h	Disable non-maskable interrupt (NMI)
04h	Get processor type
06h	Initialize system hardware
08h	Initialize chipset with initial POST values
09h	Set IN POST flag
0Ah	Initialize CPU registers
0Bh	Enable CPU cache
0Ch	Initialize caches to initial POST values
0Eh	Initialize I/O component
0Fh	Initialize the local bus IDE
10h	Initialize power management
11h	Load alternate registers with initial POST *valuesnew*
12h	Restore CPU control word during warm boot
13h	Initialize PCI bus mastering devices
14h	Initialize keyboard controller
16h	BIOS ROM checksum
17h	Initialize cache before memory autosize
18h	8254 timer initialization
1Ah	8237 DMA controller initialization
1Ch	Reset programmable interrupt controller
20h	Test DRAM refresh
22h	Test keyboard controller
24h	Set ES segment register to 4 GB
26h	Enable A20 line
28h	Autosize DRAM
29h	Initialize POST memory manager

continued

Table 68. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
2Ah	Clear 512 KB base RAM
2Ch	RAM failure on address line *xxxx**
2Eh	RAM failure on data bits *xxxx** of low byte of memory bus
2Fh	Enable cache before system BIOS shadow
30h	RAM failure on data bits *xxxx** of high byte of memory bus
32h	Test CPU bus-clock frequency
33h	Initialize POST dispatch manager
34h	Test CMOS RAM
35h	Initialize alternate chipset registers
36h	Warm start shut down
37h	Reinitialize the chipset (motherboard only)
38h	Shadow system BIOS ROM
39h	Reinitialize the cache (motherboard only)
3Ah	Autosize cache
3Ch	Configure advanced chipset registers
3Dh	Load alternate registers with CMOS *valuesnew*
40h	Set Initial CPU speed new
42h	Initialize interrupt vectors
44h	Initialize BIOS interrupts
45h	POST device initialization
46h	Check ROM copyright notice
47h	Initialize manager for PCI option ROMs
48h	Check video configuration against CMOS RAM data
49h	Initialize PCI bus and devices
4Ah	Initialize all video adapters in system
4Bh	Display QuietBoot screen
4Ch	Shadow video BIOS ROM
4Eh	Display BIOS copyright notice
50h	Display CPU type and speed
51h	Initialize EISA motherboard
52h	Test keyboard
54h	Set key click if enabled
56h	Enable keyboard
58h	Test for unexpected interrupts
59h	Initialize POST display service
5Ah	Display prompt "Press F2 to enter SETUP"
5Bh	Disable CPU cache

continued

Table 68. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
5Ch	Test RAM between 512 and 640 KB
60h	Test extended memory
62h	Test extended memory address lines
64h	Jump to UserPatch1
66h	Configure advanced cache registers
67h	Initialize multiprocessor APIC
68h	Enable external and processor caches
69h	Setup System Management Mode (SMM) area
6Ah	Display external L2 cache size
6Ch	Display shadow-area message
6Eh	Display possible high address for UMB recovery
70h	Display error messages
72h	Check for configuration errors
74h	Test real-time clock
76h	Check for keyboard errors
7Ah	Test for key lock on
7Ch	Set up hardware interrupt vectors
7Eh	Initialize coprocessor if present
80h	Disable onboard Super I/O ports and IRQs
81h	Late POST device initialization
82h	Detect and install external RS232 ports
83h	Configure non-MCD IDE controllers
84h	Detect and install external parallel ports
85h	Initialize PC-compatible PnP ISA devices
86h	Re-initialize onboard I/O ports
87h	Configure motherboard configurable devices
88h	Initialize BIOS Data Area
89h	Enable Non-Maskable Interrupts (NMIs)
8Ah	Initialize extended BIOS data area
8Bh	Test and initialize PS/2 mouse
8Ch	Initialize diskette controller
8Fh	Determine number of ATA drives
90h	Initialize hard-disk controllers
91h	Initialize local-bus hard-disk controllers
92h	Jump to UserPatch2
93h	Build MPTABLE for multiprocessor boards
94h	Disable A20 address line (Rel. 5.1 and earlier)
95h	Install CD-ROM for boot

continued

Table 68. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
96h	Clear huge ES segment register
97h	Fix up multiprocessor table
98h	Search for option ROMs
99h	Check for SMART Drive
9Ah	Shadow option ROMs
9Ch	Set up power management
9Eh	Enable hardware interrupts
9Fh	Determine number of ATA and SCSI drives
A0h	Set time of day
A2h	Check key lock
A4h	Initialize typematic rate
A8h	Erase F2 prompt
Aah	Scan for F2 key stroke
Ach	Enter SETUP
Aeh	Clear IN POST flag
B0h	Check for errors
B2h	POST done - prepare to boot operating system
B4h	One short beep before boot
B5h	Terminate QuietBoot
B6h	Check password (optional)
B8h	Clear global descriptor table
B9h	Clean up all graphics
Bah	Initialize DMI parameters
BBh	Initialize PnP Option ROMs
BCh	Clear parity checkers
BDh	Display MultiBoot menu
Beh	Clear screen (optional)
BFh	Check virus and backup reminders
C0h	Try to boot with INT 19h
C1h	Initialize POST Error Manager (PEM)
C2h	Initialize error logging
C3h	Initialize error display function
C4h	Initialize system error handler

continued

Table 68. Port 80h Codes (continued)

Code	Description of POST Operation (The following are for boot block in flash ROM)
E0h	Initialize the chipset
E1h	Initialize the bridge
E2h	Initialize the processor
E3h	Initialize system timer
E4h	Initialize system I/O
E5h	Check force recovery boot
E6h	Checksum BIOS ROM
E7h	Go to BIOS
E8h	Set huge segment
E9h	Initialize multiprocessor
Eah	Initialize OEM special code
Ebh	Initialize PIC and DMA
Ech	Initialize memory type
Edh	Initialize memory size
Eeh	Shadow boot block
Efh	System memory test
F0h	Initialize interrupt vectors
F1h	Initialize runtime clock
F2h	Initialize video
F3h	Initialize beeper
F4h	Initialize boot
F5h	Clear huge segment
F6h	Boot to mini-DOS
F7h	Boot to full DOS

* If the BIOS detects error 2C, 2E, or 30 (base 512 K RAM error), it displays an additional word-bitmap (xxxx) indicating the address line or bits that failed. For example, "2C 0002" means address line 1 (bit one set) has failed. "2E 1020" means data bits 12 and 5 (bits 12 and 5 set) have failed in the lower 16 bits. The BIOS also sends the bitmap to the port-80 LED display. It first displays the check point code, followed by a delay, the high-order byte, another delay, and then the low-order byte of the error. It repeats this sequence continuously.

5.3 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem. The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (no card installed or faulty) or if an external ROM module does not properly checksum to zero.

An external ROM module (e.g., video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST Terminal Error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video, and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 69. Beep Codes

Beeps	Port 80h Code	Explanation
1-2-2-3	16h	BIOS ROM checksum
1-3-1-1	20h	Test DRAM refresh
1-3-1-3	22h	Test keyboard controller
1-3-3-1	28h	Autosize DRAM
1-3-3-2	29h	Initialize POST memory manager
1-3-3-3	2Ah	Clear 512 KB base RAM
1-3-4-1	2Ch	RAM failure on address line xxxx
1-3-4-3	2Eh	RAM failure on data bits xxxx of low byte of memory bus
1-4-1-1	30h	RAM failure on data bits xxxx of high byte of memory bus
2-1-2-2	45h	POST device initialization
2-1-2-3	46h	Check ROM copyright notice
2-2-3-1	58h	Test for unexpected interrupts
2-2-4-1	5Ch	Test RAM between 512 and 640 KB
1-2	98h	Search for option ROMs. One long, two short beeps on checksum failure.

6 Customer Support and Specifications

6.1 Online Support

Find information about Intel boards under “Product Info” or “Customer Support” at this World Wide Web site:

http://support.intel.com/support/motherboards/desktop/

6.2 Specifications

The motherboard complies with specifications listed in Table 70.

Table 70. Compliance with Specifications

Specification	Description	Revision Level
AC ’97	Audio Codec ’97 Component Specification	Revision 2.1, May 22, 1998, Intel Corporation. This specification is available at: http://developer.intel.com/pc-supp/platform/ac97/.
ACPI	Advanced Configuration and Power Interface specification	Revision 1.0a, July 1, 1998, Intel Corporation, Microsoft Corporation, and Toshiba Corporation. The specification is available at: http://www.teleport.com/~acpi/
AGP	Accelerated Graphics Port Interface Specification (1X and 2X)	Revision 2.0, May 4, 1998, Intel Corporation. The specification is available through the Accelerated Graphics Implementers Forum at: http://www.agpforum.org/.
APM	Advanced Power Management BIOS interface specification	Revision 1.2, February, 1996, Intel Corporation and Microsoft Corporation.
ATA-3	Information Technology - AT Attachment-3 Interface	X3T10/2008D Revision 6. The specification is available at the ATA Anonymous FTP Site: fission.dt.wdc.com.
ATAPI	ATA Packet Interface for CD-ROMs	SFF-8020i Revision 2.5. (SFF) Fax Access: (408) 741-1600.
ATX	ATX form factor specification	Revision 2.01, February 1997, Intel Corporation. The specification is available at: http://developer.intel.com/design/motherbd/atx.htm.

continued

Table 70. Compliance with Specifications (continued)

Specification	Description	Revision Level
El Torito	Bootable CD-ROM format specification	Version 1.0, January 25, 1995 Phoenix Technologies Ltd., and IBM Corporation. The El Torito specification is available on the Phoenix Web site at: http://www.ptltd.com/products/specs.html.
EPP	Enhanced Parallel Port	IEEE 1284 standard, Mode [1 or 2], v1.7.
IrDA	Serial Infrared Physical Layer Link specification	Version 1.1, October 17, 1995 Infrared Data Association.
PCI	PCI Local Bus Specification PCI Power Management Interface Specification	Revision 2.1, June 1, 1995, PCI Special Interest Group. Revision 1.0, June 30, 1997, PCI Special Interest Group. These specifications can be ordered at: http://www.pcisig.com/.
Phoenix BIOS	Phoenix BIOS	Revision 4.0, February 27, 1997, Phoenix Technologies Ltd.
Plug and Play	Plug and Play BIOS specification	Version 1.0a, May 5, 1994 Compaq Computer Corporation, Phoenix Technologies Ltd., and Intel Corporation.
SDRAM DIMMs (64-and 72-bit)	PC SDRAM Unbuffered DIMM Specification PC SDRAM DIMM Specification PC Serial Presence Detect (SPD) Specification	Revision 1.0, February , 1998, Intel Corporation. Revision 1.63, October, 1998, Intel Corporation. Revision 1.2A, December, 1997, Intel Corporation. These specifications are available at: http://developer.intel.com/design/pcisets/memory/.
SMBIOS	System Management BIOS Reference Specification	Version 2.3, August 12, 1998, American Megatrends Inc., Award Software International Inc., Compaq Computer Corporation, Dell Computer Corporation, Hewlett-Packard Company, Intel Corporation, Phoenix Technologies Ltd., and SystemSoft Corporation. The specification is available at: http://developer.intel.com/ial/WfM/design/smbios/.
USB	Universal serial bus specification	Revision 1.1, September 23, 1998 Compaq Computer Corporation, Digital Equipment Corporation, IBM PC Company, Intel Corporation, Microsoft Corporation, NEC, and Northern Telecom. This specification is available at: http://www.usb.org/developers/.