Enterprise Server Group

Intel R440LX DP Server Baseboard
Technical Product Specification

Preliminary

Released version 0.1
Order Number:
July, 1997

The R440LX DP Server baseboard may contain design defects or errors known as errata. Characterized errata that may cause the R440LX DP Server baseboard's behavior to deviate from published specifications are documented in the R440LX DP Server Specification Update.

Revision History

Revision	Revision History	Date
Rev 0.1	Initial release of the R440LX DP Server Baseboard Technical Product Specification	7/97

This product specification applies only to standard R440LX DP Server board set with BIOS identifier **XXX**. Information in this version of the summary applies to the BIOS **XXXXXXX** . Different versions of the BIOS may look and behave differently.

***NOTE**: If printing this document from an electronic file, use a PostScript printer with the appropriate PostScript print driver to insure the drawings print clearly.*

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R440LX DP Server *BIOS External Product Specification*

Appendix A Board Set Descriptions

Product Overview

The Intel R440LX DP Server is a flat baseboard design offering a dual Pentium® II processor-based server system that combines the latest technology and integrated features to provide a high-performance platform at entry-range cost efficiency.

The R440LX DP Server baseboard utilizes the Intel 440LX AGPset, the latest in chipset technology from Intel, to maximize system performance for 32-bit application software and operating systems. The R440LX DP Server was designed to a high volume server platform with integrated features.

The R440LX DP Server design is complemented with an array of features. These include:

- *The system is fully MPS 1.4 compliant with appropriate Pentium II extensions.*
- *Memory supports up to 512MB of SDRAM memory using commodity DIMM devices.*
- *Design based on* Intel 440LX AGPset (82440LX, 82443LX PAC controller, PIIX4)
- *PCI segment: compliant with revision 2.1 of the PCI specification. PCI is provided by host bridge in the 82440LX AGPset, with 4 expansion slots.*
- *1 ISA slot and PC Compatible I/O (serial, parallel, mouse, and keyboard)*
- *Embedded PCI I/O devices, including SCSI, IDE, NIC, and Video controllers*
- *Server management features, including thermal/voltage monitoring*
- Adaptec AIC-7880 SCSI Controller
- Intel EtherExpess Pro100B 10/100 NIC
- Cirrus Logic GD5446* SVGA video
- National SuperI/O* 87307 PCI/IDE controller
- Two Single Edge Contact (S.E.C.) cartridge connectors (to accommodate dual Pentium II processors and future processor upgrades)

The R440LX DP Server baseboard supports dual 233/266/300/333/366 MHz Pentium II processors contained on Single Edge Contact (S.E.C.) cartridges. These cartridges enclose the processor with 512 KB of integrated ECC L2 cache to enable high-frequency operation. There are two S.E.C. connectors on the baseboard, with embedded VRM 8.1-compliant voltage regulator (DC-to-DC converter). The R440LX DP Server baseboard design will accommodate upgrades to future processing technology, based on the "Deschutes†".

† "Deshutes" is an Intel internal code name used to describe a processor technology that is currently under development. This code name will be replaced with an official marketing name upon release of product.

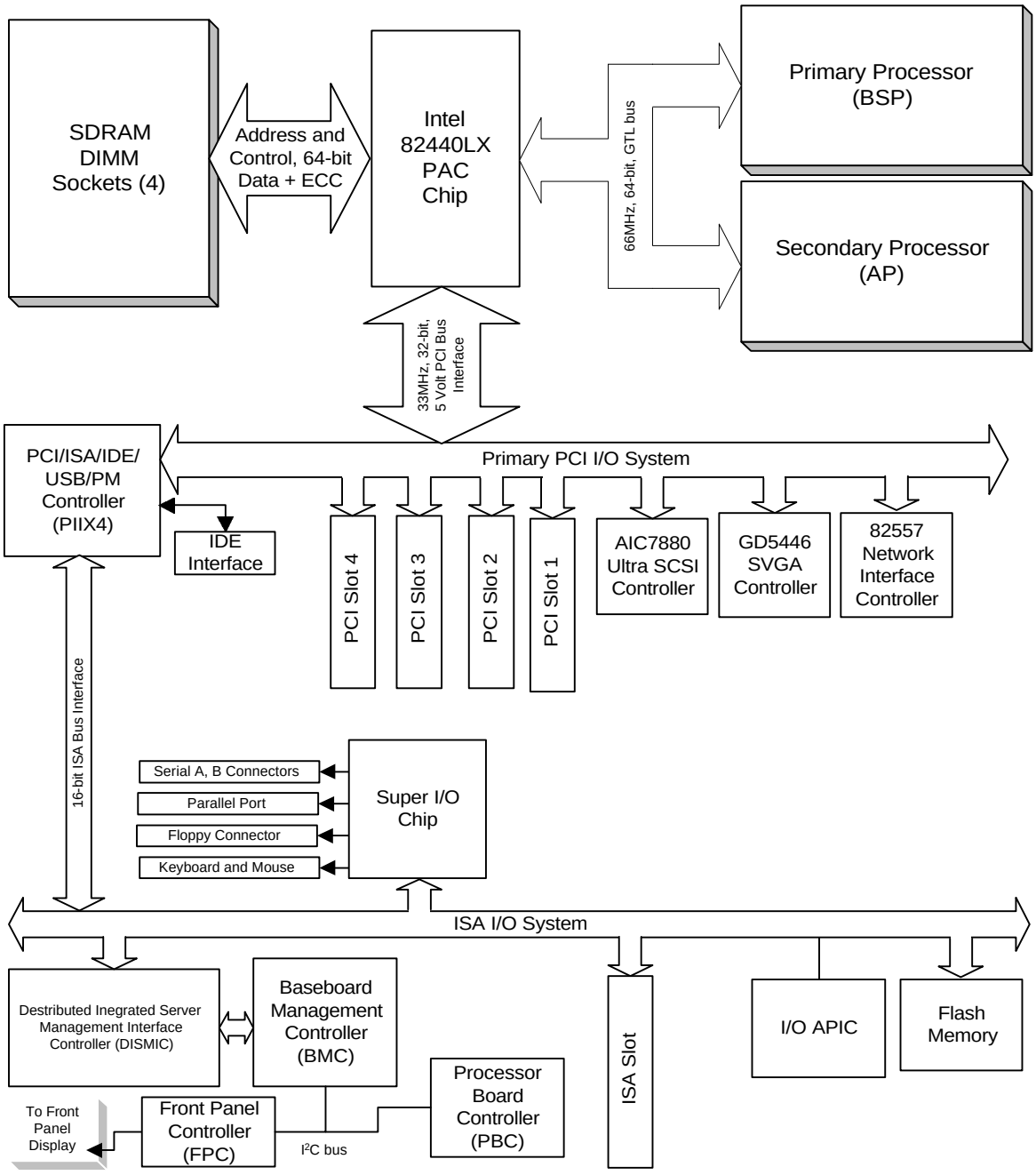

Figure 1 R440LX DP Server Functional Block Architecture

Baseboard Diagram

The following diagram shows the placement of major components and connector interfaces on the R440LX DP Server baseboard.

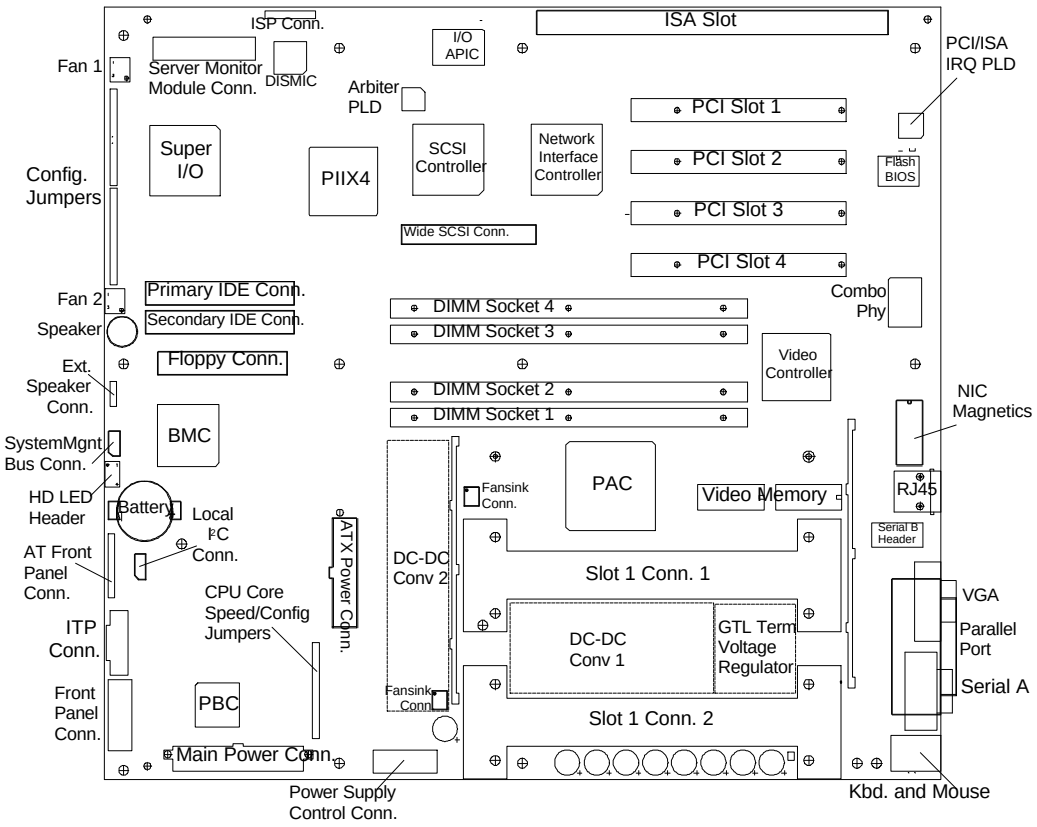

Figure 2 R440LX Baseboard Layout

Processor/PCI Host Bridge/Memory Subsystem

The processor/PCI bridge/memory subsystem consists of one or two identical Pentium II processor S.E.C. cartridges, and support circuitry on the baseboard consisting of the following:

- Intel 82443LX PCI/A.G.P. controller (PAC) PCI host bridge and memory controller
- Dual S.E.C. connectors that accept the Pentium II processor S.E.C. cartridges
- Processor host bus GTL+ support circuitry, including termination power supply
- Embedded DC-to-DC voltage converter (VRM) for both processor S.E.C. cartridges
- APIC bus
- Miscellaneous logic for reset configuration, processor S.E.C. cartridge presence detection, ITP port, and server management

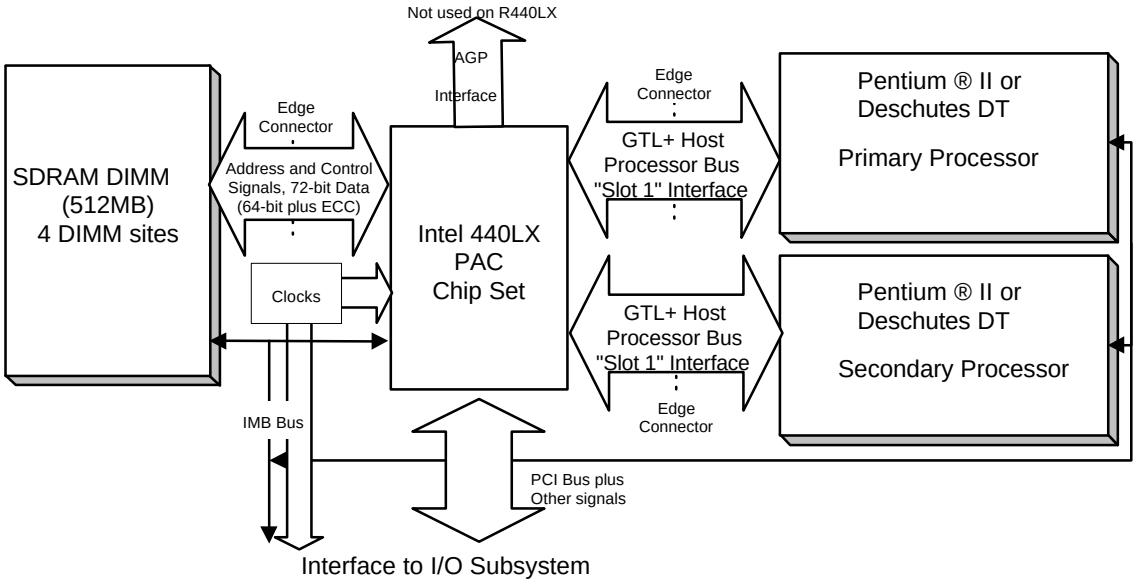

Figure 3 Processor/PCI Host Bridge/Memory Subsystem

Pentium II Processor S.E.C. Cartridge

The R440LX DP Server baseboard is designed to accommodate Pentium II processors at speeds from 233 MHz to 366 MHz. Previous Intel processors utilized technology which housed the processor core/L1 cache, and L2 cache in a dual-cavity PGA package. However, with the introduction of the Pentium II processor, the Single Edge Contact (S.E.C.) cartridge was implemented. The S.E.C. cartridge encloses the processor core/L1 cache and the L2 cache on a pre-assembled printed circuit board, approximately 2.5" x 5" in size.

The L2 cache and processor core/L1 cache is connected using a private bus that is isolated from the processor host bus. The Pentium II processor's L2 cache bus operates at half of the processor core frequency. To compensate for the cache bus speed, the internal L1 data and code caches have been enlarged to 16 KB.

The Pentium II processor S.E.C. cartridge's external interface is designed to be MP-ready. Each processor contains a local APIC section for interrupt handling. When two S.E.C. cartridges are installed, they must be of identical revision, core voltage, and bus/core speeds.

Retention Module

The Pentium II processor retention module is used to add stability to the S.E.C. connector and a way of providing attachment to the baseboard.

Cartridge Connector

The Pentium II processor S.E.C. connector conforms to the “Slot 1” specification, which can also accommodate future processor S.E.C. cartridges. The baseboard provides two connectors. The processors face towards the DIMM memory.

Processor Bus Termination/Regulation/Power

The termination circuitry required by the Pentium II processor bus (GTL+) signaling environment and the circuitry to set the GTL+ reference voltage, are implemented directly on the S.E.C. cartridges. The baseboard provides 1.5V GTL+ termination power (VTT), and VRM 8.1-compliant DC-to-DC converters to provide processor power (VCCP) at each connector. Power for primary processor is derived from the +12V supply, and the secondary processor utilizes th +5V supply using an embedded DC-DC converter onboard. A socket is provided on the baseboard for a VRM to power processor 1, which derives power from the 5V supply.

Termination Card

Logic is provided on the baseboard to detect the presence and identity of installed processor or termination cards. If only one Pentium II processor S.E.C. cartridge is installed in a system, a termination card *must* be installed in the vacant S.E.C. connector to ensure reliable system operation. The termination card contains GTL+ termination circuitry, clock signal termination, and Test Access Port (TAP) bypassing for the vacant connector. The R440LX DP server supports termination’s cards with VID bit 11111 or 01110.

APIC Bus

Interrupt notification and generation for the Pentium II processors is done using an independent path between local APICs in each processor and the Intel I/O APIC located on the baseboard. This simple bus consists of two data signals and one clock line. Refer to the *I/O APIC and Interrupts* section later in this chapter for more information.

440LX Host Bridge

The 82443LX PCI/A.G.P. controller (PAC) is the host bridge between the Pentium II processors and I/O systems. The 82443LX PAC is a 492-pin ball-grid array (BGA) device that performs control signal translations and manages the data path. The host bridge in the PAC supports one or two processors at a processor host bus frequency of 66 MHz, with 32-bit addressing, optimized in-order and request queue (IOQ), and dynamic deferred transaction support. The GTL+ host bus connects the processor cartridge with other resources in the system through the 440LX PAC host bridge. The host bridge translates 64-bit operations in the GTL+ signaling environment at 66 MHz to a 32-bit PCI I/O subsystem.

The PCI interface provides greater than 100 MB/s data streamlining for PCI to DRAM accesses, while supporting concurrent processor host bus and PCI transactions to main memory. This is accomplished using extensive data buffering, with processor-to-DRAM and PCI-to-DRAM write data buffering and write-combining support for processor-to-PCI burst writes. The PCI bus supports eight PCI masters: NIC, PCI slots 1 through 4, SCSI, PIIX4, and PAC). Note that the PCI video is a slave only device, and does not require PCI bus mastership. All PCI masters must arbitrate for PCI access, using resources supplied by both the PAC and the added Arbitration logic.

The 440LX PAC also contains the memory controller for R440LX. Memory amounts from 32 MB to 512 MB of DIMM is possible, with a 64/72-bit non-interleaved pathway to SDRAM main memory.

ECC is provided which can detect and correct single-bit errors (SED/SEC), and detect all double-bit and some multiple-bit errors (DED). Under configuration (F1 Setup or SCU) control, you may configure parity checking, and the level of ECC desired. On power-up ECC and parity checking are disabled.

PCI I/O Subsystem

All I/O for R440LX DP Server, including PCI and PC-compatible, is directed through PCI. The R440LX DP Server PCI bus supports the following embedded devices and connectors:

- Four 120-pin, 32-bit PCI expansion slot connectors
- PIIX4 PCI-to-ISA bridge and IDE controller
- PCI video controller, Cirrus Logic CL-GD5446
- PCI Ultra SCSI Controller, Adaptec AIC-7880
- PCI Network Interface Controller, Intel 82557

Each device under the PCI host bridge has its IDSEL signal connected to one bit out of the PCI Address/Data lines **AD[31::11]**, which acts as a device select on the PCI bus. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached, along with its corresponding device number. Refer to "Accessing Configuration Space" in Chapter 4 for more information.

IDSEL Value	Device
20	PCI Slot 0
21	PCI Slot 1
22	SCSI
23	PCI Slot 2
26	PCI Slot 3
27	NIC
29	Video
31	PIIX4

Table 1 PCI Configuration IDs

PCI Arbitration

The R440LX DP Server PCI bus supports eight PCI masters: NIC, PCI slots 1 through 4, SCSI, PIIX4, and PAC). All PCI masters must arbitrate for PCI access, using resources supplied by both the PAC and the added Arbitration logic. Note that the PCI video is a slave only device, and does not require PCI bus mastership. The host bridge PCI interface arbitration lines **REQ_L** and **GNT_L** are a special case in that they are internal to the host bridge. PIIX4 arbitration signals are also a special case so that access time capability for ISA masters is guaranteed. Because the primary PCI bus supports six PCI masters (slots P0 through P2, i960 RD, SCSI, PIIX4, and PAC) and one slave, all PCI masters must arbitrate for PCI access. The 440LX PAC accomplishes this. Note that the PCI video is a slave only device

PCI-to ISA/IDE/USB Controller (PIIX4)

The PIIX4 provides four specific PCI functions in a single package, PCI-to-ISA bridge, IDE interface, USB controller (not used on the R440LX), and power management controller. Each of the 4 functions in the PIIX4 contain its own set of configuration registers that appear to the R440LX system as a unique hardware controller sharing the same PCI bus interface.

The PIIX4 is packaged as a 324-pin BGA device

The PIIX4 fully implements a 32-bit PCI master/slave interface, in accordance with the *PCI Local Bus Specification, Rev. 2.1*. The PCI interface operates at 33 MHz, using the 5V-signaling environment.

The PIIX4 provides an ISA bus interface, operating at 8.33 MHz, that supports a single ISA connector, Flash memory, server management interface, and the National Super I/O chip.

The Fast IDE controller in the PIIX4 supports programmed I/O transfers up to 14 MB/s and bus master IDE transfers up to 32 MB/s on two IDE channels.

SCSI Subsystem

The R440LX DP Server baseboard provides an embedded SCSI host adapter: Adaptec AIC-7880. The AIC-7880 contains a SCSI controller with full-featured PCI bus master interface in a BGA package. The 7880 supports either 8- or 16-bit Fast SCSI providing 10 MB/s or 20 MB/s (Fast-10) throughput, or Fast-20 SCSI that can burst data at 20 MB/s or 40 MB/s. As a PCI 2.1 bus master the AIC-7880 supports burst data transfers on PCI up to the maximum rate of 133 MB/sec using the on-chip 256 byte FIFO. The 7880 also offers active negation outputs, controls for external differential transceivers, a disk activity output, and a SCSI terminator powerdown control. Active negation outputs reduce the chance of data errors by actively driving both polarities of the SCSI bus, avoiding indeterminate voltage levels and common-mode noise on long cable runs. The SCSI output drivers can directly drive a 48 mA single-ended SCSI bus with no additional drivers (the SCSI segment can handle up to 15 devices). SCSI termination power is always on, regardless of the register settings for 7880 SCSI termination power control features. The embedded SCSI controller on Redwood always sits at one end of the SCSI bus.

Adaptec AIC-7880 PCI Signals

The AIC-7880 supports all of the required 32-bit PCI signals including the PERR_L and SERR_L functions. Full PCI parity is maintained on the entire data path through the chip. The device also takes advantage of PCI interrupt signaling capability, which is hardwired to PCI_INTC_L on the R440LX DP Server baseboard. The figure below shows the PCI signals supported by the AIC-7880.

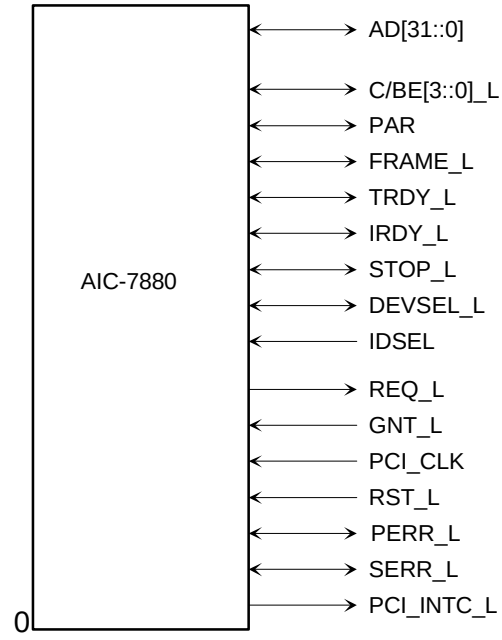

Figure 4 Embedded SCSI PCI Signals

PCI Video

R440LX DP Server has a Cirrus Logic CL-GD5446 integrated video controller and support circuitry on the PCI bus. The CL-GD5446 32-bit VGA Graphics Accelerator chip contains a SVGA video controller, Clock Generator, and 80 MHz RAMDAC. Two 256 K x 16 EDO DRAM chips provide 1 MB of 60 ns video memory. The 5446 supports a variety of modes: up to 1280 x 1024 resolution, and up to 64 K colors.

This SVGA subsystem supports analog VGA monitors, single and multi-frequency, interlaced and non-interlaced, up to 87 Hz vertical retrace frequency. The connector is a standard 15 pin VGA connector.PCI Video

The R440LX DP Server will only support 1MB of Video memory and is not expandable.

Video Chip PCI Signals

The CL-GD5446 supports a minimal set of 32-bit PCI signals since it never acts as a PCI master. As a PCI slave, the device requires no arbitration or interrupt connections.

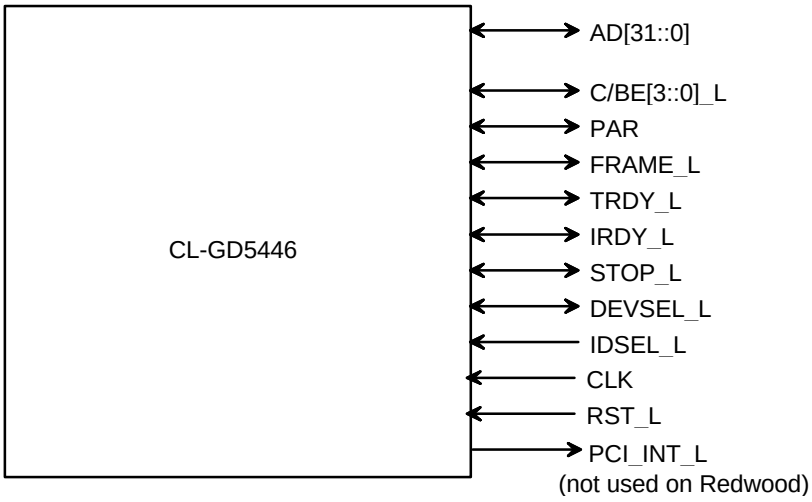

Figure 5 Video Controller PCI Signals

Video Controller PCI Commands

The CL-GD5446 supports the following PCI commands:

Table 2 Video Chip Supported PCI Commands

		CL-GD5446 Support	
C/BE[3::0]_L	**Command Type**	**Target**	**Master**
0000	Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read	Yes	No
0011	I/O Write	Yes	No
0100	Reserved	No	No
0101	Reserved	No	No
0110	Memory Read	Yes	No

0111	Memory Write	Yes	No
1000	Reserved	No	No
1001	Reserved	No	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	No	No
1101	Dual Address Cycle	No	No
1110	Memory Read Line	No	No
1111	Memory Write and Invalidate	No	No

Video Modes

The CL-GD5446 supports all standard IBM VGA modes. With 1 MB of video memory, R4 edwood goes beyond standard VGA support. The following tables show the standard and extended modes that the chip supports, including the number of colors and palette size (e.g., 16 colors out of 256 K colors), resolution, pixel frequency, and scan frequencies.

Table 3 Standard VGA Modes

Mode(s) in Hex	Bits Per Pixel	Colors (number /palette size)	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
0, 1	4	16/256K	360 X 400	14	31.5	70
2, 3	4	16/256K	720 X 400	28	31.5	70
4, 5	4	4/256K	320 X 200	12.5	31.5	70
6	4	2/256K	640 X 200	25	31.5	70
7	4	Mono	720 X 400	28	31.5	70
D	4	16/256K	320 X 200	12.5	31.5	70
E	4	16/256K	640 X 200	25	31.5	70
F	4	Mono	640 X 350	25	31.5	70
10	4	16/256K	640 X 350	25	31.5	70
11	4	2/256K	640 X 480	25	31.5	60
12	4	16/256K	640 X 480	25	31.5	60
12+	4	16/256K	640 X 480	31.5	37.5	75
13	8	256/256K	320 X 200	12.5	31.5	70
14, 55	8	16/256K	1056 X 400	41.5	31.5	70
54	8	16/256K	1056 X 350	41.5	31.5	70
58, 6A	8	16/256K	800 X 600	40	37.8	60
58, 6A	8	16/256K	800 X 600	49.5	46.9	75
5C	8	256/256K	800 X 600	36	35.2	56
5C	8	256/256K	800 X 600	40	37.9	60
5C	8	256/256K	800 X 600	49.5	46.9	75
5D	8	16/256K (interlaced)	1024 X 768	44.9	35.5	87
5D	8	16/256K	1024 X 768	65	48.3	60
5D	8	16/256K	1024 X 768	75	56	70
5D	8	16/256K	1024 X 768	78.7	60	75
5F	8	256/256K	640 X 480	25	31.5	60
5F	8	256/256K	640 X 480	31.5	37.5	75
60	8	256/256K (interlaced)	1024 X 768	44.9	35.5	87
60	8	256/256K	1024 X 768	65	48.3	60
60	8	256/256K	1024 X 768	75	56	70
60	8	256/256K	1024 X 768	78.7	60	75

64	16	64K	640 X 480	25	31.5	60
64	16	64K	640 X 480	31.5	37.5	75
Mode(s) in Hex	**BPP**	**Colors**	**Resolution**	**Pixel Freq. (MHz)**	**Horiz. Freq. (KHz)**	**Vert. Freq. (Hz)**
65	16	64K	800 X 600	36	35.2	56
65	16	64K	800 X 600	40	37.8	60
65	16	64K	800 X 600	49.5	46.9	75
66	16	32K Direct/256 Mixed	640 X 480	25	31.5	60
66	16	32K Direct/256 Mixed	640 X 480	31.5	37.5	75
67	16	32K Direct/256 Mixed	800 X 600	40	37.8	60
67	16	32K Direct/256 Mixed	800 X 600	49.5	46.9	75
6C	16	16/256K (interlaced)	1280 X 1024	75	48	87

For more information refer to the *Cirrus Logic CL-GD5446 Reference Manual, Cirrus Logic CL-GD5446 Advance Product Bulletin*

VGA connector

The following table shows the pinout of the VGA connector:

Table 4 Video Port Connector Pinout

Pin	Signal	Description
1	RED	Analog color signal R
2	GREEN	Analog color signal G
3	BLUE	Analog color signal B
4	nc	No connect
5	GND	Video ground (shield)
6	GND	Video ground (shield)
7	GND	Video ground (shield)
8	GND	Video ground (shield)
9	nc	No connect
10	GND	Video ground
11	nc	No connect
12	DDCDAT	Monitor ID data
13	HSYNC	Horizontal Sync
14	VSYNC	Vertical Sync
15	DDCCLK	Monitor ID clock

For more information refer to the *Cirrus Logic CL-GD5446 Reference Manual* or *Cirrus Logic CL-GD5446 Advance Product Bulletin*.

ISA I/O Subsystem

On R440LX DP Server, the PIIX4 provides a bridge to an ISA I/O subsystem, that supports the following connectors and devices:

- 1 ISA slot
- Flash memory for BIOS ROM and extensions
- National Semiconductor PC87307VUL Super I/O chip, which supports the following:
  - ⇒ 2 PC-compatible serial ports

- ⇒ Enhanced parallel port
- ⇒ Floppy controller
- ⇒ Keyboard/Mouse ports

The ISA I/O subsystem also connects with the Intel I/O APIC, interrupt rerouter, and DISMIC. The I/O APIC handles interrupts produced by ISA devices for the multiprocessor environment. The DISMIC is a programmable logic device that provides the host interface to the baseboard server management processor, and performs NMI and SMI control. Refer to “Interrupts and I/O APIC” later in this chapter for more information on these devices and how they are used in the Redwood interrupt structure.

I/O Controller Subsystem

The Super I/O device contains all of the necessary circuitry to control two serial ports, one parallel port, floppy disk, and PS/2-compatible keyboard and mouse. Redwood provides the connector interface for each. In addition, the Super I/O contains a real-time clock, which is unused on Redwood.

Serial Ports

Two 9-pin D-Sub connectors are provided, one in the stacked housing for Serial port A and the second via an on-board header for Serial port B. Both ports are compatible with 16550A and 16450, and are relocatable. Each serial port can be set to 1 of 4 different COM ports, and can be enabled separately. When enabled, each port can be programmed to generate edge or level sensitive interrupts. When disabled, serial port interrupts are available to add-in cards. The pinout for the two connectors is shown below:

Table 5 Serial Port A Connector Pinout

Pin	Name	Description
1	DCD	Data Carrier Detected
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Ground
6	DSR	Data Set Ready
7	RTS	Return to Send
8	CTS	Clear to Send
9	RIA	Ring Indication Active

Table 6 Serial Port B Header Connector Pinout

Pin	Name	Description
1	DCD	Data Carrier Detected
2	DSR	Data Set Ready
3	RXD	Receive Data
4	RTS	Return to Send
5	TXD	Transmit Data
6	CTS	Clear to Send
7	DTR	Data Terminal Ready
8	RIA	Ring Indication Active
9	GND	Ground
10	nc	-

Parallel Port

The 25/15 pin high rise connector stacks the parallel port connector over the VGA and serial Port A connector. The 87307 provides an IEEE 1284-compliant 25-pin bi-directional parallel port. BIOS programming of the Super I/O registers enable the parallel port, and determine the port address and interrupt. When disabled, the interrupt is available to add-in cards. Pinout is shown below:

Table 7 Parallel Port Connector Pinout

Pin	Name	Pin	Name
1	STROBE_L	14	AUFDXT_L
2	D0	15	ERROR_L
3	D1	16	INIT_L
4	D2	17	SLCTIN_L
5	D3	18	GND
6	D4	19	GND
7	D5	20	GND
8	D6	21	GND
9	D7	22	GND
10	ACK_L	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT		

Floppy Disk Controller

The FDC on the Super I/O is functionally compatible with the PC8477, which contains a superset of the floppy disk controllers in the DP8473 and N82077. The baseboard provides the 24 MHz clock, termination resistors, and chip selects. All other FDC functions are integrated into the Super I/O, including analog data separator and 16-byte FIFO. The floppy disk connector on the baseboard has the following pinout:

Table 8 Floppy Port Connector Pinout

Pin	Name	Pin	Name
1	GND	18	FD_DIR_L
2	FD_DENSEL	19	GND
3	GND	20	FD_STEP_L
4	nc	21	GND
5	Key	22	FD_WDATA_L
6	FD_DRATE0	23	GND
7	GND	24	FD_WGATE_L
8	FD_INDEX_L	25	GND
9	GND	26	FD_TRK0_L
10	FD_MTR0_L	27	FD_MSEN0
11	GND	28	FD_WPROT_L
12	FD_DR1_L	29	GND
13	GND	30	FD_RDATA_L
14	FD_DR0_L	31	GND
15	GND	32	FD_HDSEL_L
16	FD_MTR1_L	33	GND
17	FD_MSEN1	34	FD_DSKCHG_L

Keyboard and Mouse Connectors

The keyboard and mouse connectors are mounted within a single stacked housing. The mouse connector is stacked over the keyboard connector. External to the board they appear as two connectors. The keyboard and mouse controller are software compatible with the 8042AH and PC87911. The keyboard and mouse connectors are PS/2 compatible, with pinout shown below:

Table 9 Keyboard Connector Pinout

Pin	Signal	Description
1	KEYDAT	Keyboard Data
2	(NC)	
3	GND	Ground
4	FUSED_VCC	+5 V, fused
5	KEYCLK	Keyboard Clock
6	(NC)	

Table 10 Mouse Connector Pinout

Pin	Signal	Description
1	MSEDAT	Mouse Data
2	(NC)	
3	GND	Ground
4	FUSED_VCC	+5 V, fused
5	MSECLK	Mouse Clock
6	(NC)	

Real-time Clock

This feature is not used on Redwood. The PIIX4 performs this function.

General Purpose I/O

In addition to the dedicated features, the PC87307VUL has sixteen available general purpose I/O, and three available programmable chip selects. The following tables describe the use of these ports.

Table 11 General Purpose Chip Select Assignment

Signal	Description	Address Range
CS0_L	Unused	
CS1_L	Unused	
CS2_L	Unused	

Table 12 General Purpose I/O Assignment

Signal	Name	Description
GPIO10		Unused.
GPIO11		Unused.
GPIO12		Unused.
GPIO13		Unused.
GPIO14		Unused.
GPIO15		Unused.
GPIO16		Unused.
GPIO17		Unused.
GPIO20	EXT_SMI_EN_L	Enables SDRAM ECC errors to generate SMIs
GPIO21	BMC_SMI_EN_L	Enables BMC to generate SMIs
GPIO22	PERR_SMI_EN_L	Enables PCI PERR to generate SMIs
GPIO23		Unused.
GPIO24		Unused.
GPIO25		Unused.
GPIO26		Unused.
GPIO27		Unused.

System Reset Control

Reset circuitry on the R440LX DP Server baseboard monitors reset from the front panel, PIIX4, I/O controller, and processor subsystem to determine proper reset sequencing for all types of reset. The reset logic is designed to accommodate a variety of ways to reset the system, which can be divided into the following categories:

- Power-up reset
- Hard reset
- Soft (programmed) reset

Power-up Reset

Power-up reset occurs on the initial application of power to the system. The power supply asserts its "power good" signal within 400 to 2000ms of its output voltages being stable. The Front Panel Controller (FPC) monitors this signal, and asserts its power good output 30 to 40ms after detecting the power supply's power good signal asserted (the onboard VRMs are designed to provide stable CPU power 30 to 40ms after the main power is stable).

Hard Reset

Hard reset may be initiated by software, or by the user resetting the system through the front panel. For software initiated hard reset, the PIIX4 Reset Control register should be used. The front panel reset is routed to the PIIX4 through the reset and power microcontroller. Both sources of hard reset cause the PIIX4 to assert ISA bus reset (**RST_RSTDRV**) and PCI reset (**RST_P_RST_LB**). **RST_RSTDRV** resets the ISA subsystem, while **RST_P_RST_L** resets the PCI bus. The 440LX receives the PCI reset signal and propagates it to the processor subsystem

Soft Reset

Soft resets may be generated by the keyboard controller (**RST_KB_L**), or by the chipset in the processor subsection (**RST_INIT_REQ_L**). The two sources of soft reset are combined in the reset logic, and routed to the processor subsection via the **RST_INIT_CPU_L** signal. Soft reset causes the processors to begin execution in a known state without flushing caches or internal buffers.

A programmed reset may be initiated by software. Although reset control is provided by registers in the PAC, the 82440LX documentation recommends that the PIIX4 Reset Control register be used instead for programmed resets. Refer to the 82*440LX Host Bridge* or *PAC Component Specification* for more information.

Reset Diagram

Reset flows throughout the R440LX DP Server baseboard as shown in the following figure.

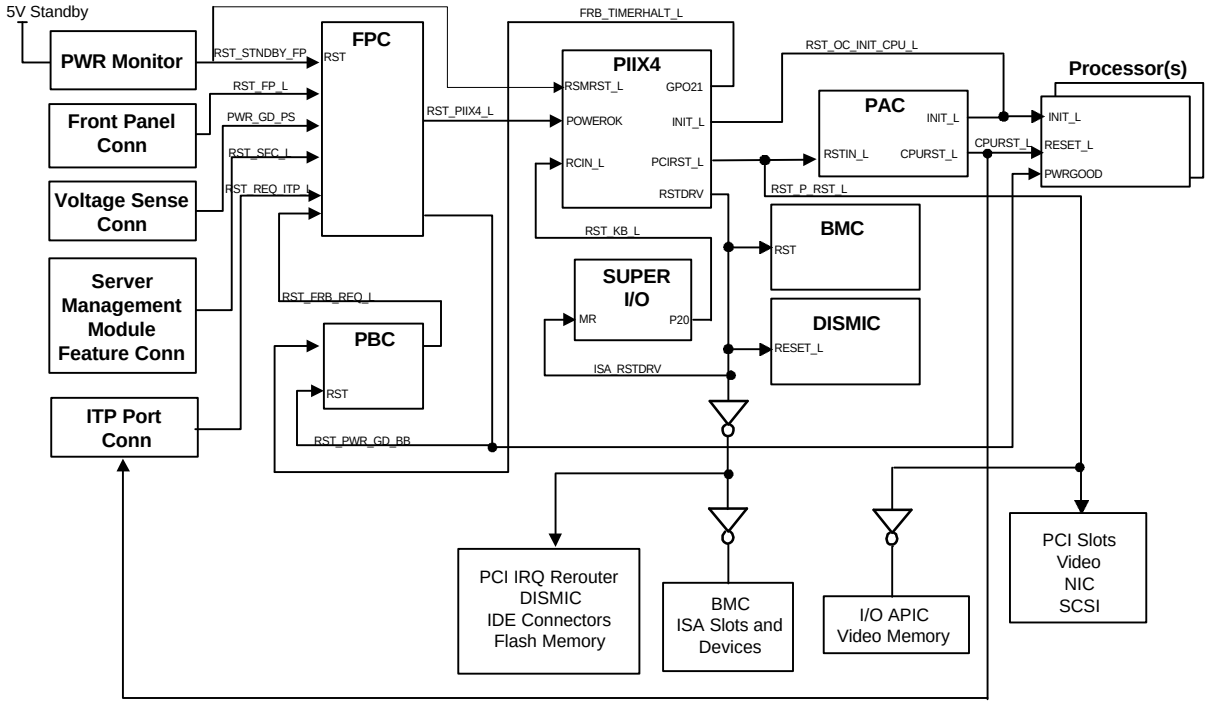

Figure 6 Reset Flow Diagram

Clock Generation and Distribution

For information on clock generation, refer to the *Mixed Voltage Clock Synthesizer/Driver Specification with SDRAM Support*. All buses on Redwood operate using synchronous clocks. The clock synthesizer on the memory board generates clock frequencies and voltage levels required by the processor subsystem, including the following:

- 66.6 MHz at 2.5V logic levels - Both Slot 1 connectors, the 82440LX, the ITP port
- 66.6 MHz at 3.3V logic levels - SDRAM DIMMs
- 33.3 MHz at 3.3V logic levels - Reference clock for the PCI bus clock driver
- 14.31818 MHz at 2.5V logic levels - Processor and I/O APIC bus clock

There are three clock sources used on the Redwood baseboard. The first source is the CPU Clock Generator, which generates the 33.3 MHz PCI reference clock, the 66.6 MHz host clocks, and the 14.318 MHz APIC clocks. A second clock source, the I/O Clock Generator, generates a 40 MHz clock for the embedded SCSI controller, a 24 MHz clock for the Super I/O, one 12 MHz clock each for the BMC and PBC, a 48MHz clock for the USB (USB is not implemented on Redwood), and a 14.318 MHz clock for ISA devices. The Front Panel Controller has its own 12 MHz crystal, as it does not run from the main 5V VCC. The following figure illustrates clock generation and distribution on the Redwood baseboard.

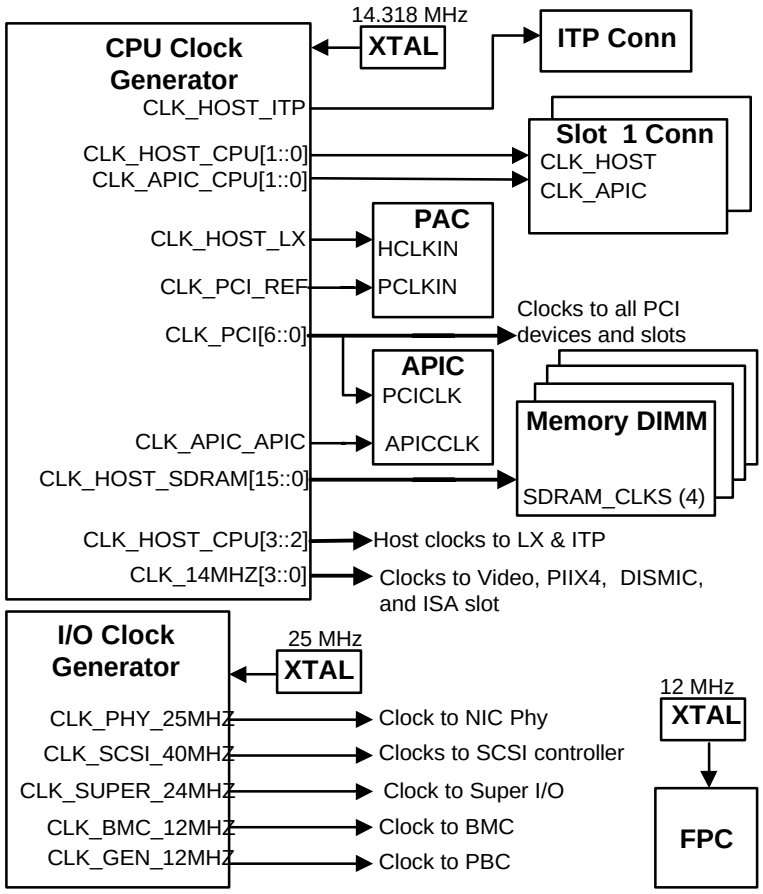

Figure 7 Redwood Baseboard Clock Distribution

Interrupts and I/O APIC

Redwood interrupt architecture accommodates both PC-compatible PIC mode, and dual-processor APIC mode interrupts. In addition, Redwood provides a PCI to ISA interrupt rerouting mechanism for compatibility with some multiprocessor operating systems which do not fully support the APIC.

PIIX4 Compatibility Interrupt Controller

For PC-compatible mode, the PIIX4 provides two 82C59-compatible interrupt controllers embedded in the device. The two controllers are cascaded with interrupt levels 8-15 entering on level 2 of the primary interrupt controller (standard PC configuration). A single interrupt signal is presented to the processors, to which only one processor will respond for servicing. The PIIX4 and Super I/O contain configuration registers that define which interrupt source logically maps to I/O APIC INTx pins. In PIC mode, the PIIX4 provides a way to direct PCI interrupts onto one of the interrupt request levels 1-15. Note that this is only useful in compatibility mode since the redirected interrupts are not sourced on the outputs of the PIIX4.

Intel I/O APIC

For APIC mode, R440LX DP Server interrupt architecture incorporates the Intel I/O APIC device, to manage and broadcast interrupts to local APICs in each processor. The I/O APIC monitors interrupt requests from devices, and on occurrence of an interrupt sends a message corresponding to the interrupt via the APIC bus to the CPU's local APIC. The APIC bus minimizes interrupt latency time for compatibility interrupt sources, in both single and dual processor operation. The I/O APIC can also supply greater than 16 interrupt levels to the processor(s). This APIC bus consists of an APIC clock, and two bi-directional data lines.

R440LX DP Server APIC structure consists of a single I/O APIC device with 24 input interrupt requests. Compatibility interrupt levels 0 through 15 appear on inputs 0 through 15. The I/O APIC also manages 8 interrupt levels associated with PCI interrupts: PCI interrupts A through D are routed to APIC inputs 16 through 19. This supports more efficient interrupt processing. The PIIX4 also contains I/O APIC features that are not used in the R440LX DP Server platform.

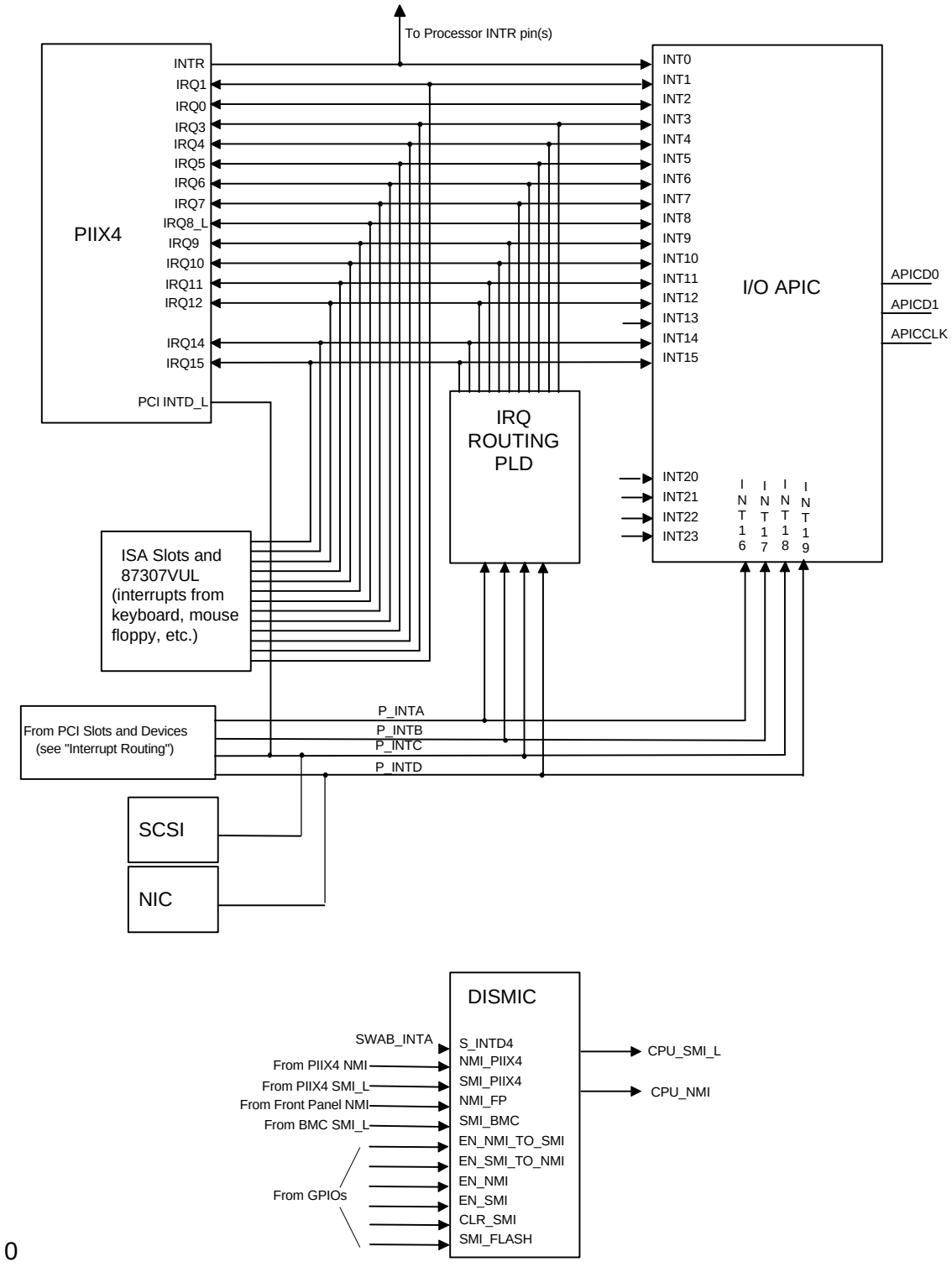

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Figure 8 Redwood Interrupt Structure

Interrupt Sources

The following table recommends the logical interrupt mapping of interrupt sources on Redwood. The actual interrupt map is defined using configuration registers in the PIIX4 and the I/O controller. I/O Redirection Registers in the I/O APIC are provided for each interrupt signal, which define hardware interrupt signal characteristics for APIC messages sent to local APIC(s). Use the information provided in this table to determine how to program each interrupt.

Table 13 Interrupt Definitions

Interrupt	I/O APIC level	Description
INTR	INT0	Processor interrupt
NMI		NMI from DISMIC to processor
IRQ1	INT1	Keyboard interrupt
Cascade	INT2	Interrupt signal from second 8259 in PIIX4
IRQ3	INT3	Serial port A or B interrupt from 87307VUL device, user-configurable.
IRQ4	INT4	Serial port A or B interrupt from 87307VUL device, user-configurable.
IRQ5	INT5	
IRQ6	INT6	Floppy disk
IRQ7	INT7	Parallel port
IRQ8_L	INT8	RTC interrupt
IRQ9	INT9	
IRQ10	INT10	
IRQ11	INT11	
IRQ12	INT12	Mouse interrupt
	INT13	
IRQ14	INT14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1
IRQ15	INT15	
PCI_INTA_L	INT16	PCI Interrupt signal A
PCI_INTB_L	INT17	PCI Interrupt signal B
PCI_INTC_L	INT18	PCI Interrupt signal C
PCI_INTD_L	INT19	PCI Interrupt signal D
SMI_L		System Management Interrupt. General-purpose error indicator from a control PAL that provides an SMI_L from non-traditional error sources (PERR_L, SERR_L, and others).

PCI Add-in Card Slot Interrupt Sharing

The following figure shows how PCI interrupts, shared between slots and embedded controllers, are cascaded to avoid conflicts (since most PCI cards use PCI_INTA_L as their interrupt pin). The arrows indicate the direction of interrupt flow from slot to slot, with final destination at the PIIX4 interrupt inputs.

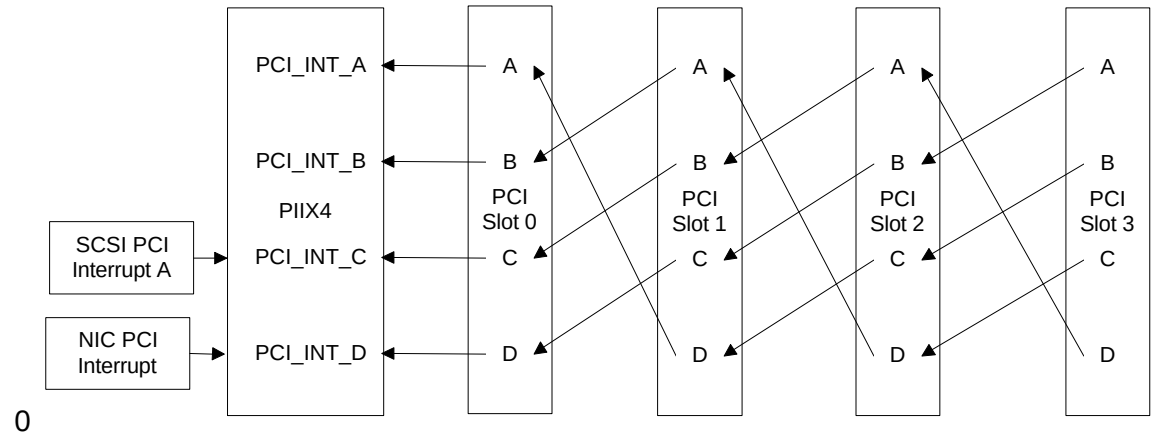

Figure 9 PCI Slot Interrupt Swizzle

PCI Interrupt Rerouting

Some multiprocessor operating systems are unable to handle interrupts from PCI slots and devices as pure PCI interrupts, via inputs 16-19 (allocated to PCI) of the I/O APIC. Rather, they expect PCI interrupts to be delivered as ISA IRQs. Multiprocessor operating systems may also expect some interrupts from the PC-compatible PIC in the PIIX4, and others from the I/O APIC (Mixed Mode). Some device drivers check whether the device uses one of the traditional IRQs, and if not (when the PCI interrupt is connected directly to the I/O APIC), the driver fails to install or run properly. The PIIX4 performs internal PCI to IRQ interrupt steering so that PCI interrupts can be delivered to the PIC. However, the PCI interrupt steering feature is unidirectional, which means that it cannot redirect PCI interrupts to the I/O APIC.

For these reasons, R440LX DP Server incorporates an external PCI to IRQ rerouter circuit, that can be programmed to pass PCI interrupts through to inputs 16-19 of the I/O APIC, or deliver a specific PCI interrupt to an ISA IRQ. Under software control, a PCI interrupt can be individually rerouted to an ISA IRQ signal.

Two 8-bit registers are provided in the rerouter circuit, with each nibble of a register controlling a specific PCI Interrupt line via PIO commands. The PIIX4 decodes the address of the PIO command and produces a chip select, which is controlled using the PIIX4 Programmable Chip Select Control register (78h - 79h). The rerouter uses only 2 bytes of the minimum 4 selectable, so aliases are provided.

System Board Jumpers

Two 15-pin single inline headers provide eight 3-pin jumper blocks that control various configuration options, as shown in the figure below. The shaded areas show default jumper placement for each configurable option

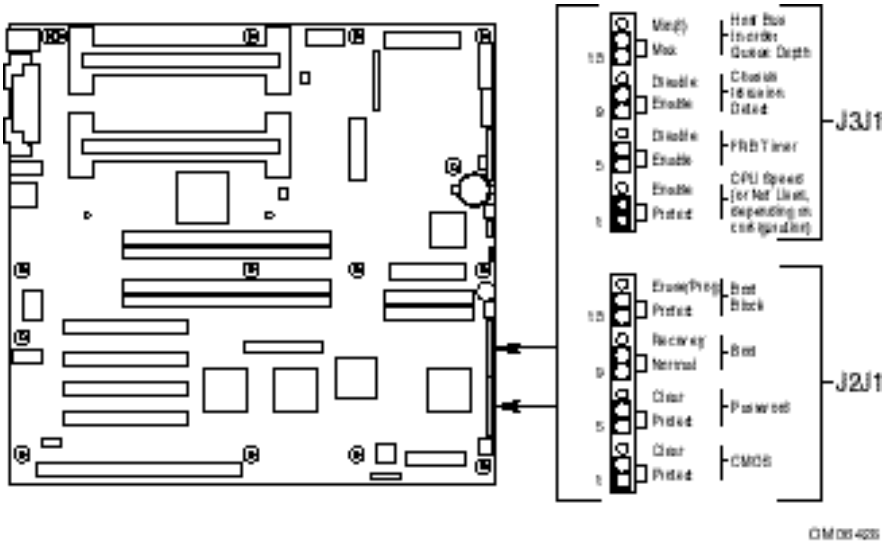

Figure 10 Board Jumper location

Table 14 Board Jumper discription

Function	Pins (default in bold)	What it does at system reset
CMOS clear	**1-2, Protect**	Preserves the contents of NVRAM.
	2-3, Erase	Replaces the contents of NVRAM with the manufacturing default settings.
Password clear	**5-6, Protect**	Maintains the current system password.
	6-7, Erase	Clears the password.
Recovery Boot	**9-10, Normal**	System attempts to boot using the BIOS stored in flash memory.
	10-11, Recovery	BIOS attempts a recovery boot, loading BIOS code from a floppy diskette into the flash device. This is typically used when the BIOS code has been corrupted.
Boot Block Write Protect	**13-14, Protect**	BIOS boot block is write-protected
	14-15	BIOS boot block is erasable and programmable
		⚠ **CAUTION** Programming the boot block incorrectly will prevent the system from booting.
CPU Speed	**1-2, Protect**	Processor speed configuration is protected.

	2-3, Enable	Processor speed configuration is enabled. **Note** Depending on your configuration, this jumper is either available to set the speed of the processor, or not available at all.
FRB Timer Enable	**5-6, Enable**	FRB operation is enabled (system boots from processor 1 if processor 0 fails)..
	6-7, Disable	FRB is disabled..
Chassis Intrusion Detection	**9-10, Enable**	Switch installed on chassis indicates when cover has been removed.
	10-11, Disable	Chassis intrusion switch is bypassed.
Host Bus In-order Queue	**13-14, Max**	Host in-order queue depth is set at maximum.
	14-15, Min (1)	Host in-order queue depth is set at 1 (used for debugging).

Appendix B Server Management

The baseboard contains three microcontrollers that control the server management features on the baseboard, as part of a private I^2C-based communications network that extends throughout the server chassis and beyond. The Baseboard Management Controller (BMC) is the primary controller, monitoring and logging key events as well as passing messages to the other distributed microcontrollers in the system. The BMC interfaces to the ISA bus via a programmable logic component, the Distributed Integrated Server Management & Interface Controller (DISMIC). The Front Panel Controller (FPC) controls the reset and power on/off circuitry on the baseboard, and interfaces to the BMC via the I^2C bus. The Processor Board Controller (PBC) monitors processor board temperature and voltages, controls Fault-Resilient Booting (FRB), and provides the interface to the module serial number and board ID information. It can be polled for current status, or configured to automatically send an alert message when an error condition is detected. The PBC also uses the I^2C bus for communication with the baseboard.

Server Management

R440LX DP Server server management architecture features 3 microcontrollers for server management and monitoring as shown in the following figure:

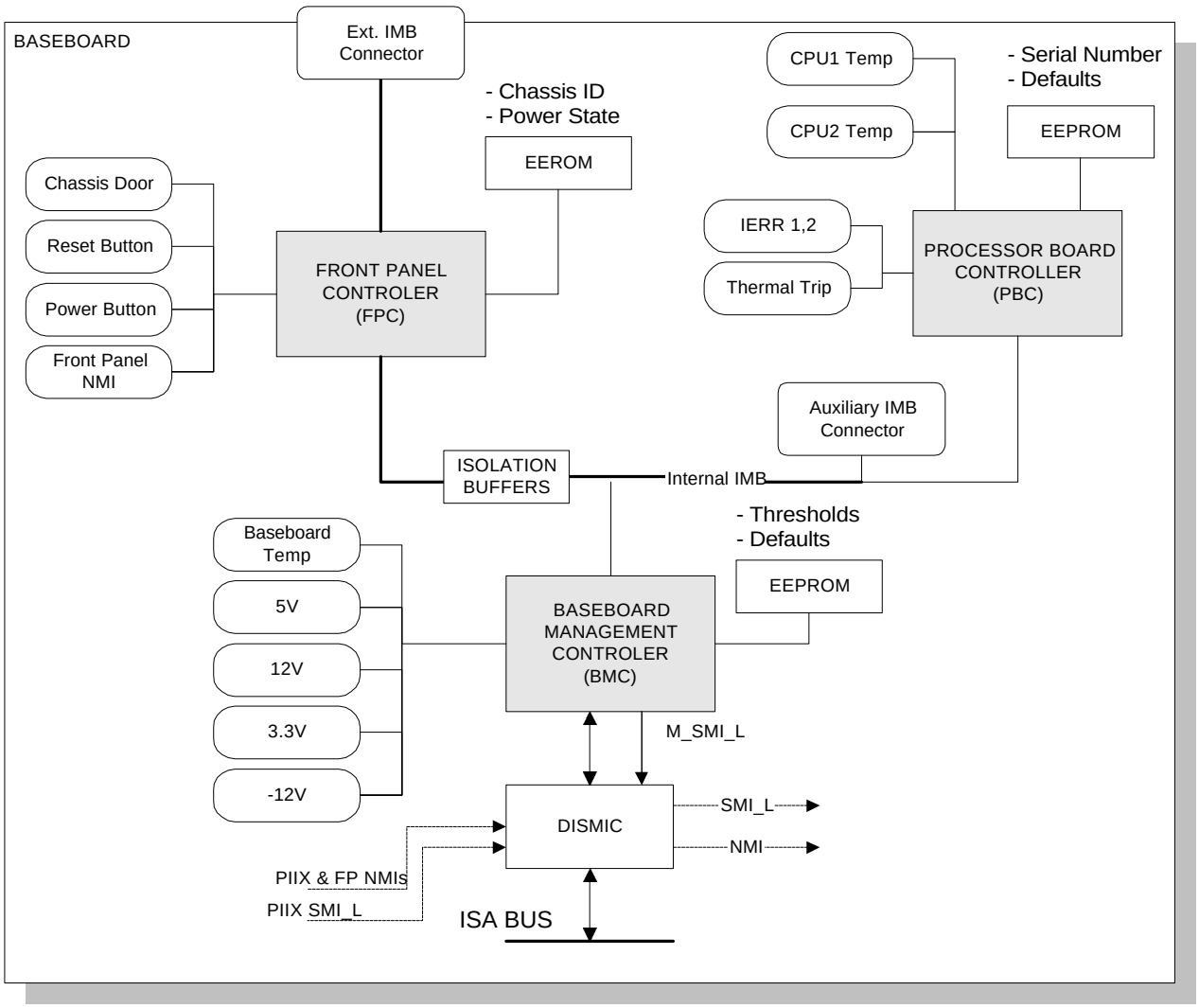

Figure 11 R440LX DP Server Management Block Diagram

A shared register interface is defined for control of server management functions.

Server Management Controllers

Three microcontrollers are provided on R440LX DP Server for server management and monitoring functions:

- Front Panel Controller (FPC)
- Processor Board Controller (PBC)
- Baseboard Management Processor (BMC)

Baseboard Management Controller (BMC)

The BMC is an 8051-compatible microcontroller located on the R440LX DP Server baseboard. The BMC directly monitors baseboard power supply and SCSI termination voltages using an onboard Analog to Digital Converter (ADC), and checks the status of the fan fail indicators. The BMC also monitors system temperature sensors on the Intelligent Management Bus. When any monitored parameter is outside defined thresholds, the BMC generates an SMI. The BMC also provides general purpose I/O (GPIO) functions, and acts as the primary communications gateway to the FPC, PBC, and DISMIC by providing support routines for I^2C and ISA communications.

An EEPROM associated with the secondary baseboard temperature sensor contains the Chassis ID, Baseboard ID, Power State, and Baseboard Temperature during power-off conditions. These values are managed by the BMC via I^2C. For more information on BMC functionality, refer to the *BMC Interface Specification* for R440LX DP Server.

Processor Board Controller (PBC)

The PBC monitors processor voltage levels, processor thermal trip and internal error signals. It can be polled for current status, or configured to automatically send an alert message when an error condition is detected. The PBC implementation was used from the B440FX DP server and kept the same name, there is not a processor board on the R440LX DP Server.,

Front Panel Controller (FPC)

The FPC manages front panel system power on/off control, system reset, and NMI buttons, along with the external IMB interface. The device is powered from the +5V Standby, to stay alive when the power is switched off to the rest of the baseboard. The FPC controls main power to the baseboard and is responsible for monitoring all sources of power control both on and off the baseboard including the Front Panel, Server Monitor Module, PIIX4, and RTC power control signals. The FPC retains the current power state if main power is momentarily lost.

The FPC also detects chassis intrusion by monitoring an external switch via a front panel board or the baseboard chassis intrusion connector.

Fault Resilient Booting

The PBC implements Fault Resilient Booting (FRB) levels 1, 2, and 3. If two processors are installed and the processor designated as the BSP fails to complete the boot process, FRB attempts to boot the system using the alternate processor.

- FRB level 1 is for recovery from a BIST failure detected during POST. This FRB recovery is fully handled by BIOS code.
- FRB level 2 is for recovery from a Watchdog timeout during POST. The Watchdog timer for FRB level 2 detection is implemented in the PBC.
- FRB level 3 is for recovery from a Watchdog timeout on Hard Reset / Power-up. Hardware functionality for this level of FRB is provided by the BMC on the processor subsystem.

FRB-3 is managed by the PBC, which controls the ability to boot using either processor in the event of a catastrophic processor failure. On power up, a timer starts that can only be stopped by a healthy processor using the GPIO bit, FRB_TMRHLT_L, on the PIIX4. If the primary processor fails to halt the FRB timer before timeout, the controller asserts STOP_FLUSH to the processor and asserts FRB_RST_L for 10ms. When the system comes out of reset, the primary processor is unable to act as the BSP allowing the other processor to take over the boot process.

IMB Isolation Buffers and Auxiliary IMB Connector

Buffers are provided to isolate the baseboard temperature sensors, auxiliary IMB connector, and FPC from the rest of the IMB bus. These buffers, running on the standby supply, keep the bus alive to the FPC even though main power is switched off. This allows the FPC to communicate with its IMB EEPROM (in the secondary baseboard temperature sensor) at all times, and provides a way to remotely control power via the auxiliary IMB connector.

Table 15 Auxiliary IMB Connector Pinout

Pin	Signal
1	Local IMB SCL
2	GND
3	Local IMB SDA

WARNING!

A shorted I^2C connection at the auxiliary IMB connector will prevent restoration of main power.

Server Monitor Module Connector

The Server Monitor Module feature connector is supported on the baseboard. Several of the undefined connector pins have been allocated for 2 IEEE 1149.1 channels. The pinout of the 26-pin connector is shown in the following table.

Table 16 Server Monitor Module Connector Pinout

Pin	Signal	Description
1	CPU_SMI_L	System Management Interrupt
2	LOCAL_I2C_SCL	I^2C clock line
3	GND	Ground
4	Reserved	-
5	PWR_CNTRL_SFC_L	Host power supply on/off control
6	LOCAL_I2C_SDA	I^2C serial data line
7	5VSTNDBY	+5V standby indication (power OK)
8	KEYLOCK_SFC_L	Keyboard lock signal
9	CPU_NMI	Non-maskable interrupt indication
10	VCC3	3.3V power supply status input
11	RST_SFC_L	Baseboard reset signal from Server Monitor Module
12	GND	Ground
13	GND	Ground

Pin	Signal	Description
14	Reserved	-
15	SECURE_MODE_BMC	Secure mode indication
16	GND	Ground
17	SFC_CHASSIS_INSTRUSION_L	Chassis intrusion indication
18	Reserved	-
19	Reserved	-
20	GND	Ground
21	Reserved	-
22	Reserved	-
23	Reserved	unused
24	Reserved	-
25	Key pin (nc)	Connector key
26	Reserved	-

System Fan Interface

The R440LX DP Server baseboard provides four 3-pin, shrouded, and keyed fan connectors. Two of these connectors, located next to each Pentium II processor cartridges on the baseboard, are for a fansink. The remaining two connectors on the baseboard attach to chassis fans equipped with a sensor that indicates whether the fan is operating. The sensor pins for these fans are routed to the BMC for failure monitoring. The two connector types have the following pinout:

Table 17 Chassis Fan Connector Pinout

Pin	Signal
1	GND
2	Fan Sensor
3	+12V

Table 18 Fansink Connector Pinout

Pin	Signal
1	GND
2	+12V
3	Fan Sensor

Appendix C Memory and Other Resource Mappings

This chapter describes the initial programming environment including address maps for memory and I/O, techniques and considerations for programming ASIC registers, and hardware options configuration. **Refer to Chapter 5 for definitions of configuration and I/O registers.**

Memory Space

At the highest level, Pentium II processor address space is divided into 4 regions, as shown in the following figure. Each region contains subregions, as described in following sections. Attributes can be independently assigned to regions and subregions using PAC registers.

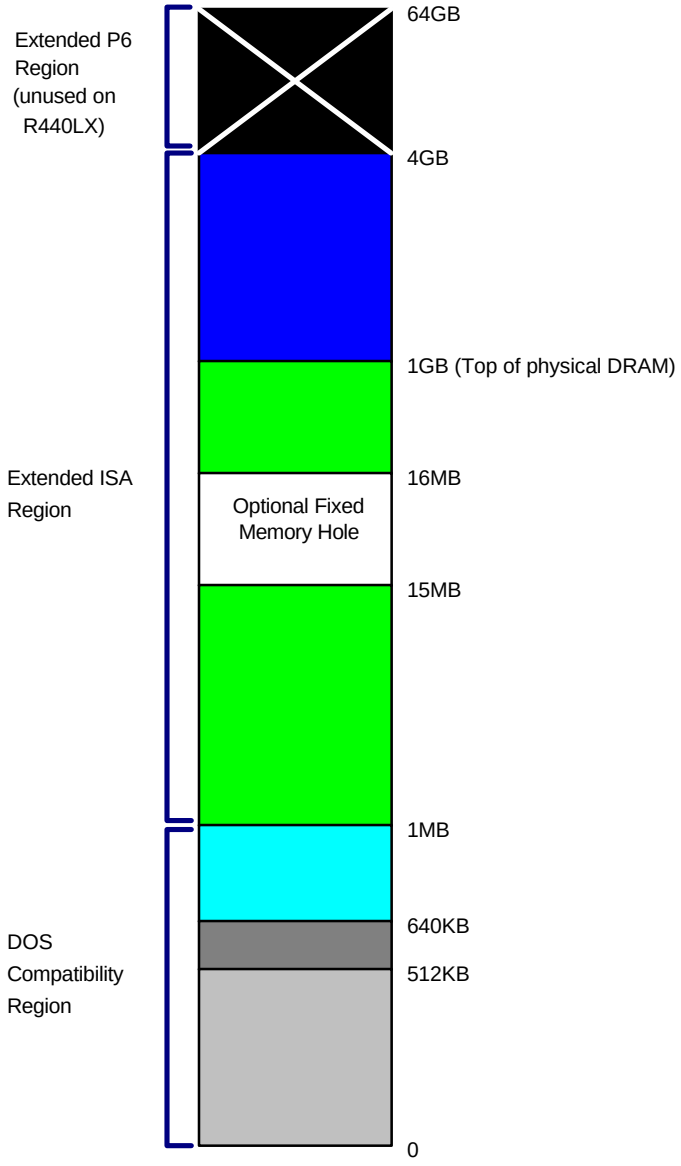

Figure 12 Pentium® II Processor Memory Address Space

DOS Compatibility Region

The first region of memory below 1 MB was defined for early PCs, and must be maintained for compatibility reasons. This region is divided into sub-regions as shown in the following figure.

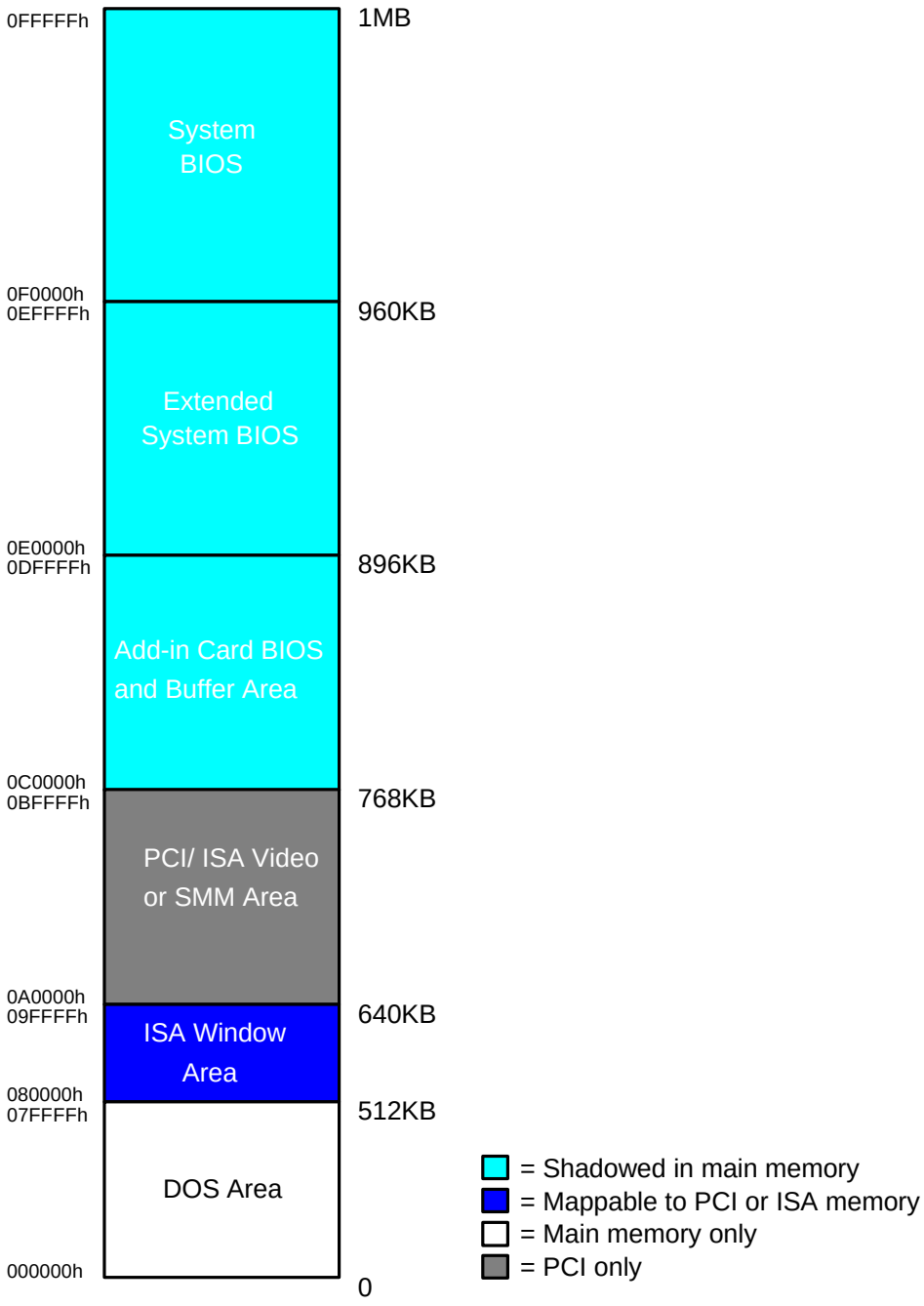

Figure 13 DOS Compatibility Region

DOS Area

The DOS region is 512 KB in the address range 0 to 07FFFFh. This region is fixed and all accesses go to main memory.

ISA Window Memory

The ISA Window Memory is 128 KB between the addresses of 080000h to 09FFFFh. This area can be mapped to the PCI bus or main memory.

Video or SMM Memory

The 128 KB Graphics Adapter Memory region at 0A0000h to 0BFFFFh is normally mapped to the VGA controller on the PCI bus. This region is also the default region for SMM space. The SMM region can be remapped by programming the SMRAM Control Register in the PAC.

Add-in Card BIOS and Buffer Area

The 128 KB region between addresses 0C0000h and 0DFFFFh is divided into eight segments of 16 KB segments mapped to ISA memory space, each with programmable attributes, for expansion card buffers. Historically, the 32 KB region from 0C0000h to 0C7FFFh has contained the video BIOS location on a video card. However, on R440LX DP Server, the video BIOS is located in the Extended BIOS or System BIOS areas.

Extended System BIOS

This 64 KB region from 0E0000h to 0EFFFFh is divided into 4 blocks of 16 KB each, and may be mapped with programmable attributes to map to either main memory or to the PCI bus. Typically, this area is used for RAM or ROM.

System BIOS

The 64 KB region from 0F0000h to 0FFFFFh is treated as a single block. By default this area is normally Read/Write disabled with accesses forwarded to the PCI bus. Through manipulation of R/W attributes, this region can be shadowed into main memory.

Extended Memory

Extended memory on R440LX DP Server is defined as all address space greater than 1 MB. The Extended Memory region covers 4 GB of address space from addresses 0100000h to FFFFFFFFh, as shown in the following figure.

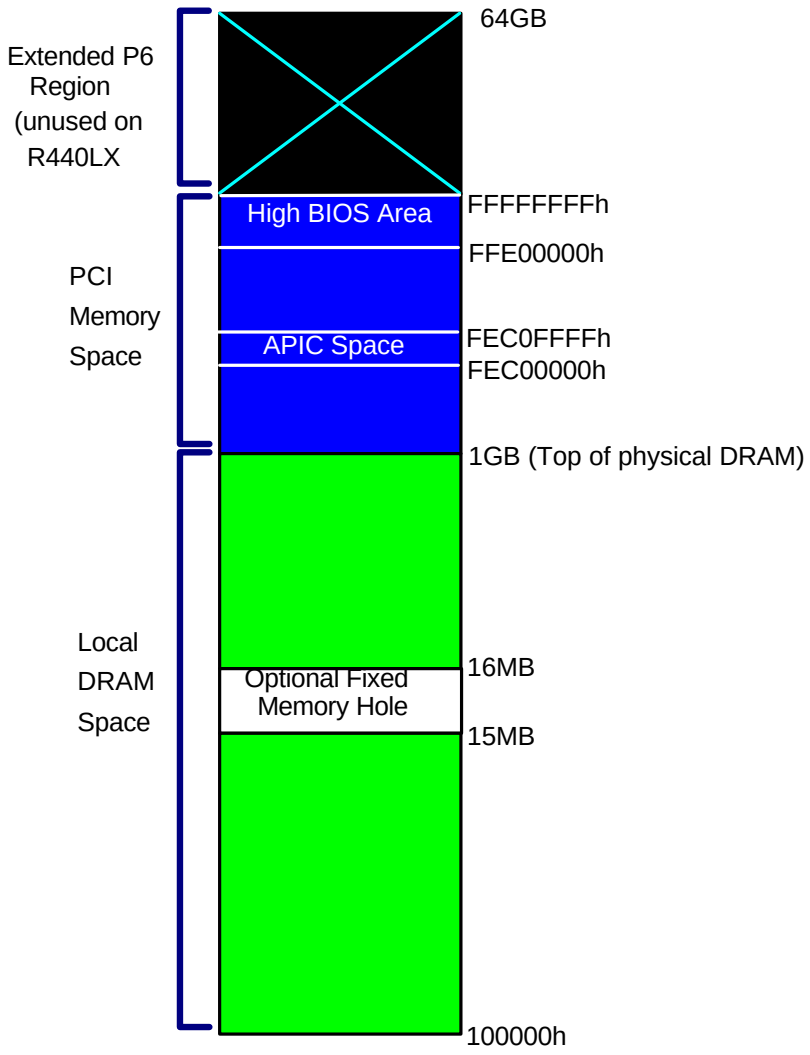

Figure 14 Extended Memory Map

Main Memory

All installed SDRAM greater than 1 MB is mapped to local main memory, up to the top of physical memory which is located at 1 GB. Memory between 1 MB to 15 MB is considered to be standard ISA extended memory. 1 MB of memory starting at 15 MB can be optionally mapped to the PCI bus memory space. **Refer to the "Fixed DRAM Hole Control" register description in Chapter 5 for details.** The remainder of this space, up to 1 GB, is always mapped to main memory.

PCI Memory Space

Memory addresses in the 1 GB to 4 GB range are mapped to the PCI bus. This region is divided into three sections: High BIOS, APIC Configuration Space, and General-purpose PCI Memory.

The General-purpose PCI Memory area is typically used for memory-mapped I/O to PCI devices. The memory address space for each device is set using PCI configuration registers

High BIOS

The top 2 MB of Extended Memory is reserved for the system BIOS, extended BIOS for PCI devices, and A20 aliasing by the system BIOS. The Pentium II processor begins executing from the High BIOS region after reset. Only 256 KB of this area is actually required by the BIOS, but 2 MB is required by Pentium II processor MTRR programming.

I/O APIC Configuration Space

A 64 KB block located 20 MB below 4 GB (0FEC00000h to 0FEC0FFFFh) is reserved for the I/O APIC configuration space.

I/O APIC units are located beginning at a base address determined by subtracting 013FFFF0h from the reset vector. The first I/O APIC is located at FEC00000h. Each I/O APIC unit is located at FEC0x000h where x is the I/O APIC unit (0 through F).

Extended Pentium® II Processor Region (above 4 GB)

A Pentium II processor-based system can have up to 64 GB of addressable memory. However, the 82440LX AGPset only supports 32-bit addressing, with the BIOS operating in 4 GB of address space (the memory DIMMs provide up to 512 MB of main memory). All accesses to the region from 4 GB to 64 GB are claimed by the PAC and terminated. Write data is dropped and zeroes are returned on reads.

Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be "shadowed" into memory located on the Pentium II processor bus. Typically, this is done to allow ROM code to execute more rapidly out of RAM. ROM is designated read-only during the copy process while RAM at the same address is designated write-only. After copying, the RAM is designated read-only and the ROM is designated write-only (shadowed). Processor bus transactions are routed accordingly. Transactions originated from the PCI bus or ISA masters and targeted at shadowed memory blocks will not appear on the processor's bus.

SMM Mode Handling

A Pentium II processor asserts SMMEM_L in its Request Phase if it is operating in System Management Mode (SMM). SM code resides in SMRAM. SMRAM can overlap with memory residing on the Pentium II processor bus or memory normally residing on the PCI bus. The PAC determines where SMRAM space is located through the value of the SMM Range configuration space register.

The SMRAM Enable bit in the SMRAM Enable configuration register determines how SM accesses are handled by the PAC. When the SMRAM Enable bit is zero (SMRAM disabled), accesses to the SMM Range with SMMEM_L asserted are ignored by the PAC. When the SMRAM Enable bit is one (SMRAM enabled), accesses to the SMM range with SMMEM_L asserted are claimed by the PAC.

If the SMMEM_L signal is not asserted, the SMM Range is not decoded regardless of the state of the SMRAM Enable bit (this allows SMRAM to overlap with memory normally residing on the processor bus).

In summary, when the SMMEM_L signal is asserted, the SMM Range is similar to a Memory Space Gap, where the SMM Enable bit either enables or disables the memory gap.

The SMI_L signal may be asserted in the Response Phase by a device in SMM power-down mode.

Refer to the System Management RAM Control Register (SMRAM 72h) **description in Chapter 5 for more information.**

I/O Map

The PAC allows I/O addresses to be mapped to the processor bus or through designated bridges in a multi-bridge system. Other PCI devices, including PIIX4, have built-in features that support PC-compatible I/O devices and functions, which are mapped to specific addresses in I/O space. On R440LX DP Server, the PIIX4 provides the bridge to ISA functions.

The I/O map in the following table shows the location in R440LX DP Server I/O space of all directly I/O-accessible registers. PCI configuration space registers for each device control mapping in I/O and memory spaces, and other features that may affect the global I/O map. All configuration space registers for PCI devices **are described in Chapter 5.** The Super I/O chip contains configuration registers that are accessed through an index and data port mechanism; these are also described in Chapter 5.

Table 19 R440LX I/O Map

Address(es)	Resource	Notes
0000h - 000Fh	DMA Controller 1	
0010h - 001Fh	DMA Controller 1	aliased from 0000h - 000Fh
0020h - 0021h	Interrupt Controller 1	
0022h - 0023h		
0024h - 0025h	Interrupt Controller 1	aliased from 0020h - 0021h
0026h - 0027h		
0028h - 0029h	Interrupt Controller 1	aliased from 0020h - 0021h
002Ah - 002Bh		
002Ch - 002Dh	Interrupt Controller 1	aliased from 0020h - 0021h
002Eh - 002Fh	Super I/O Index and Data Ports	
0030h - 0031h	Interrupt Controller 1	aliased from 0020h - 0021h
0032h - 0033h		
0034h - 0035h	Interrupt Controller 1	aliased from 0020h - 0021h
0036h - 0037h		
0038h - 0039h	Interrupt Controller 1	aliased from 0020h - 0021h
003Ah - 003Bh		
003Ch - 003Dh	Interrupt Controller 1	aliased from 0020h - 0021h
003Eh - 003Fh		
0040h - 0043h	Programmable Timers	
0044h - 004Fh		
0050h - 0053h	Programmable Timers	aliased from 0040h - 0043h
0054h - 005Fh		
0060h, 0064h	Keyboard Controller	Keyboard chip select from 87307
0061h	NMI Status & Control Register	
0063h	NMI Status & Control Register	aliased
0065h	NMI Status & Control Register	aliased
0067h	NMI Status & Control Register	aliased
0070h	NMI Mask (bit 7) & RTC Address (bits 6::0)	
0072h	NMI Mask (bit 7) & RTC Address (bits 6::0)	aliased from 0070h
0074h	NMI Mask (bit 7) & RTC Address (bits 6::0)	aliased from 0070h
0076h	NMI Mask (bit 7) & RTC Address (bits 6::0)	aliased from 0070h
0071h	RTC Data	

Redwood I/O Map (cont.)

Address(es)	Resource	Notes
0073h	RTC Data	aliased from 0071h
0075h	RTC Data	aliased from 0071h
0077h	RTC Data	aliased from 0071h
0080h - 0081h	BIOS Timer	
0080h - 008Fh	DMA Low Page Register	PIIX4
0090h - 0091h	DMA Low Page Register (aliased)	PIIX4
0092h	System Control Port A (PC-AT control Port) (this port not aliased in DMA range)	PIIX4
0093h - 009Fh	DMA Low Page Register (aliased)	PIIX4
0094h	Video Display Controller	
00A0h - 00A1h	Interrupt Controller 2	PIIX4
00A4h - 00A15	Interrupt Controller 2 (aliased)	PIIX4
00A8h - 00A19	Interrupt Controller 2 (aliased)	PIIX4
00ACh - 00ADh	Interrupt Controller 2 (aliased)	PIIX4
00B0h - 00B1h	Interrupt Controller 2 (aliased)	PIIX4
00B2h	Advanced Power Management Control	PIIX4
00B3h	Advanced Power Management Status	PIIX4
00B4h - 00B5h	Interrupt Controller 2 (aliased)	PIIX4
00B8h - 00B9h	Interrupt Controller 2 (aliased)	PIIX4
00BCh - 00BDh	Interrupt Controller 2 (aliased)	PIIX4
00C0h - 00DFh	DMA Controller 2	PIIX4
00F0h	Clear NPX error	Resets IRQ13
00F8h - 00FFh	x87 Numeric Coprocessor	
0102h	Video Display Controller	
0170h - 0177h	Secondary Fixed Disk Controller (IDE)	PIIX4 (not used)
01F0h - 01F7h	Primary Fixed Disk Controller (IDE)	PIIX4
0200h - 0207h	Game I/O Port	Not used
0220h - 022Fh	Serial Port A	
0238h - 023Fh	Serial Port B	
0278h - 027Fh	Parallel Port 3	
02E8h - 02EFh	Serial Port B	
02F8h - 02FFh	Serial Port B	
0338h - 033Fh	Serial Port B	
0370h - 0375h	Secondary Floppy	
0376h	Secondary IDE	
0377h	Secondary IDE/Floppy	
0378h - 037Fh	Parallel Port 2	
03B4h - 03BAh	Monochrome Display Port	
03BCh - 03BFh	Parallel Port 1 (Primary)	
03C0h - 03CFh	Video Display Controller	
03D4h - 03DAh	Color Graphics Controller	
03E8h - 03EFh	Serial Port A	
03F0h - 03F5h	Floppy Disk Controller	
03F6h - 03F7h	Primary IDE - Sec. Floppy	
03F8h - 03FFh	Serial Port A (Primary)	
0400h - 043Fh	DMA Controller 1, Extended Mode Registers.	PIIX4
0461h	Extended NMI / Reset Control	PIIX4

R440LX I/O Map (cont.)

Address(es)	Resource	Notes
0462h	Software NMI	PIIX4
0480h - 048Fh	DMA High Page Register.	PIIX4
04C0h - 04CFh	DMA Controller 2, High Base Register.	
04D0h - 04D1h	Interrupt Controllers 1 and 2 Control Register.	
04D4h - 04D7h	DMA Controller 2, Extended Mode Register.	
04D8h - 04DFh	Reserved	
04E0h - 04FFh	DMA Channel Stop Registers	
0678h - 067Ah	Parallel Port (ECP)	
0778h - 077Ah	Parallel Port (ECP)	
07BCh - 07BEh	Parallel Port (ECP)	
0800h - 08FFh	NVRAM	
0C80h - 0C83h	EISA System Identifier Registers	PIIX4
0C84h	Board Revision Register	
0C85h - 0C86h	BIOS Function Control	
0CA9h	DISMIC Data Register	Server management mailbox registers.
0CAAh	DISMIC Control/Status Register	
0CABh	DISMIC Flags Register	
0CF8h	PCI CONFIG_ADDRESS Register	Located in PAC
0CF9h	PAC Turbo and Reset control	PIIX4
0CFCh	PCI CONFIG_DATA Register	Located in PAC
46E8h	Video Display Controller	
xx00 - xx1F*	SCSI registers	Refer to SCSI chip doc.

*SCSI I/O base address is set using configuration registers.

Accessing Configuration Space

All PCI devices contain PCI configuration space, accessed using mechanism #1 defined in the *PCI Local Bus Specification*. The PIIX4 is accessed as a multi-function PCI device, with 3 sets of configuration registers.

If dual processors are used, only the processor designated as the BSP should perform PCI configuration space accesses. Precautions should be taken to guarantee that only one processor is accessing configuration space at a time.

Two Dword I/O registers in the PAC are used for the configuration space register access:

- CONFIG_ADDRESS (I/O address 0CF8h)
- CONFIG_DATA (I/O address 0CFCh)

When CONFIG_ADDRESS is written to with a 32-bit value selecting the bus number, device on the bus, and specific configuration register in the device, a subsequent read or write of CONFIG_DATA initiates the data transfer to/from the selected configuration register. Byte enables are valid during accesses to CONFIG_DATA; they determine whether the configuration register is being accessed or not. Only full Dword reads and writes to CONFIG_ADDRESS are recognized as a configuration access by the PAC. All other I/O accesses to CONFIG_ADDRESS are treated as normal I/O transactions.

CONFIG_ADDRESS Register

CONFIG_ADDRESS is 32 bits wide and contains the field format shown in the following figure. Bits [23::16] choose a specific bus in the system. Bits [15::11] choose a specific device on the selected bus. Bits [10::8] choose a specific function in a multi-function device. Bits [7::2] select a specific register in the configuration space of the selected device or function on the bus.

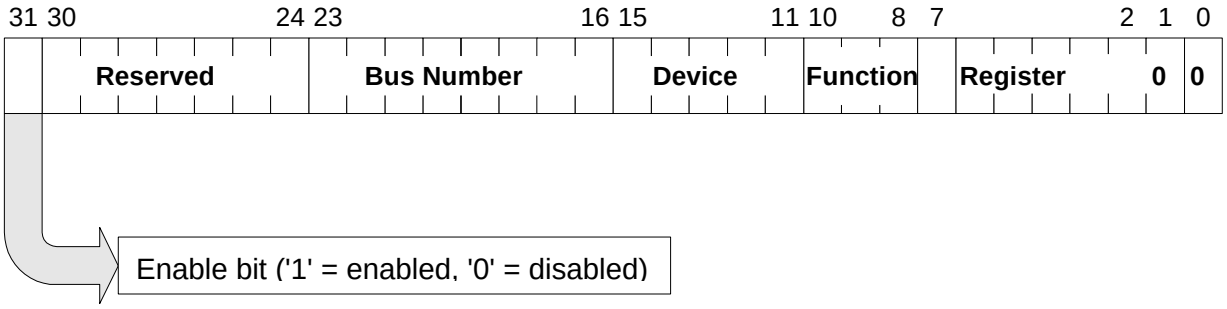

Figure 15 CONFIG_ADDRESS Register

Bus Number

PCI configuration space protocol requires that all PCI buses in a system be assigned a Bus Number. Furthermore, bus numbers must be assigned in ascending order within hierarchical buses. Each PCI bridge has registers containing its PCI Bus Number and Subordinate PCI Bus Number, which must be loaded by POST code. The Subordinate PCI Bus Number is the bus number of the last hierarchical PCI bus under the current bridge. The PCI Bus Number and the Subordinate PCI Bus Number are the same in the last hierarchical bridge.

Device Number and IDSEL Mapping

Each device under a PCI bridge has its IDSEL input connected to one bit out of the PCI bus address/data signals AD[31::11] for the PCI bus. Each IDSEL-mapped AD bit acts as a chip select for each device on PCI. The host bridge responds to a unique PCI device ID value, that along with the bus number, cause the assertion of IDSEL for a particular device during configuration cycles. The following table shows the correspondence between IDSEL values and PCI device numbers for the PCI bus. The lower 5-bits of the device number are used in CONFIG_ADDRESS bits [15::11].

Table 20 PCI Configuration IDs and Device Numbers

	PCI Bus	
IDSEL	**Device #**	**Device**
31	10100b	PIIX4
30	10011b	
29	10010b	CL-GD5446 video chip
28	10001b	
27	10000b	82557 NIC
26	01111b	PCI Slot 4

PCI Configuration IDs and Device Numbers (cont.)

IDSEL	Device #	Device
25	01110b	
24	01101b	
23	01100b	PCI Slot 3
22	01011b	Adaptec AIC-7880
21	01010b	PCI Slot 2
20	01001b	PCI Slot 1
19	01000b	
18	00111b	
17	00110b	
16	00101b	
15	00100b	
14	00011b	
13	00010b	
12	00001b	
11	00000b	Hardwired to host bridge

Error Handling

R440LX DP Server is designed to report these types of system errors: ISA bus, PCI bus, ECC memory, and System limit. Errors are reported using SMI_L. SMI is used for server management and advanced error processing. All errors can be intercepted by SMI for preprocessing (if SMI_L is enabled), or handled directly by NMI handlers. Some errors have to generate an NMI even if they are intercepted by the SMI, because the traditional way to handle errors in PC architecture is via the NMI. R440LX emulates non-ISA errors as ISA-compatible using NMI and SMI_L.

Three error handlers are required: BIOS NMI handler, OS NMI handler, and SMI handler. The SMI has the highest priority to process the errors and is OS-transparent. The OS NMI handler can process all errors as well, even when the SMI is disabled. In this case, some errors are SMI resources which can be routed to the NMI. The BIOS NMI handler processes the ISA-compatible errors and disables the NMI only.

Refer to the BIOS specification for R440LX DP Server for more information on error handling mechanisms.

Hardware Initialization and Configuration

This section describes the following:

- System initialization
- Programming considerations for various portions of the I/O system

System Initialization Sequence

A Pentium II processor system based on the 82440LX is initialized and configured in the following manner.

1. System power is applied. The power-supply provides resets using the RST_PWR_GD_BB signal. PCI reset (RST_P_RST_L) is driven to tri-state the PCI bus in order to prevent PCI output buffers from short circuiting when the PCI power rails are not within the specified tolerances. The PAC asserts G_CPURST_L to reset the processor(s).
2. The PAC is initialized, with its internal registers set to default values.
3. Before G_CPURST_L is deasserted, the PAC asserts BREQ0_L. Processor(s) in the system determine which host bus agents they are, Agent 0 or Agent 1, according whether their BREQ0_L or BREQ1_L is asserted. This determines bus arbitration priority and order.
4. The processor(s) in the system determines which processor will be the BSP by issuing Bootstrap Inter-Processor Interrupts (BIPI) on the APIC data bus. The non-BSP processor becomes an application processor and idles, waiting for a Startup Inter-Processor Interrupt (SIPI).
5. The BSP begins by fetching the first instruction from the reset vector.
6. PAC registers are updated to reflect memory configuration. SDRAM is sized and initialized.
7. All PCI and ISA I/O subsystems are initialized and prepared for booting.

Server Management Programming Interface

DISMIC mailbox registers provide a mechanism for communications between IMB server management bus agents, and SMS or SMI handler code running on the server. DISMIC mailbox register space, physically located in the device, is mapped to BMC external data memory and ISA I/O space. This shared register space consists of three byte-wide registers:

- Flags Register - provides semaphores for use in various defined operations
- Control/Status Register - accepts commands and returns completion codes
- Data Register - provides a port for transactions that exchange data

In addition to the ports described above, the DISMIC contains a port 070h snoop register. See the section titled "Port 70h Snoop Register" later in this chapter for further information.

SMS and SMI handler code interacts with the register interface using a variety of read and write commands encapsulated in messages. The origin of a message is specified during a particular transaction using Control Codes that are unique to the transaction, allowing the interface to allocate priority to various sources, and control SMI handler and SMS precedence (the SMI handler can always abort or temporarily interrupt any transaction).

Refer to the *Distributed Baseboard Management Controller Interface Specification* for more information.

Port 70h Snoop Register

The Port 70h Snoop Register reads back the state of bit 7 of I/O port 70h (RTC NMI enable bit) to the BMC. This register shadows any ISA write to port 70h. Due to architectural constraints in the DISMIC, the contents of this register cannot be made available for direct I/O read access at an alternate address location on the ISA bus. Access to the registers contents is provided only through the BMC using a command defined for this purpose.

PCI Interrupt to IRQ Routing Control

Embedded in a separate programmable logic device is logic for rerouting of PCI interrupts to ISA IRQs. Two I/O locations are reserved by the BIOS using the PIIX4 Programmable Chip Select Control register, for control of the PCI to IRQ rerouter feature: CA4h and CA5h. Writes to the upper and lower nibble of each byte determine whether the interrupt is passed through to the I/O APIC, or rerouted to an ISA IRQ input on the PIIX4. The following figure shows the PCI interrupt line associated with each nibble. The following table defines the encoding of each nibble.

A0 = 1		A0 = 0	
PCI_INTD_L	PCI_INTC_L	PCI_INTB_L	PCI_INTA_L

Bit 0

Figure 16 PCI to IRQ Rerouter Control Bytes

0Table 21 PCI to IRQ Rerouter Nibble Encoding

Value	Meaning
0000b	Pass interrupt through to I/O APIC (default)
0001b	Reserved
0010b	Reserved
0011b	Reroute PCI_INTn_L to IRQ3
0100b	Reserved
0101b	Reroute PCI_INTn_L to IRQ5
0110b	Reserved
0111b	Reroute PCI_INTn_L to IRQ7
1000b	Reserved
1001b	Reroute PCI_INTn_L to IRQ9
1010b	Reroute PCI_INTn_L to IRQ10
1011b	Reroute PCI_INTn_L to IRQ11
1100b	Reserved
1101b	Reserved
1110b	Reserved
1111b	Reroute PCI_INTn_L to IRQ15

Hardware Configuration

This section describes the jumper-configurable options on the baseboard for the following:

- System configuration
- Internal/external speaker selection

Jumper locations and designations are marked on the baseboard, refer to the layout diagram in Chapter 1 for placement information. Refer to the *R440LX DP Server BIOS EPS* for information on configuration and initialization as performed by BIOS and POST code, using configuration registers. **Refer to Chapter 5 for definitions of these registers.**

System Configuration

Two 15-pin single inline headers provide 8 3-pin jumper blocks that control various configuration options, as shown in the figure below. The shaded areas show default jumper placement for each configurable option.

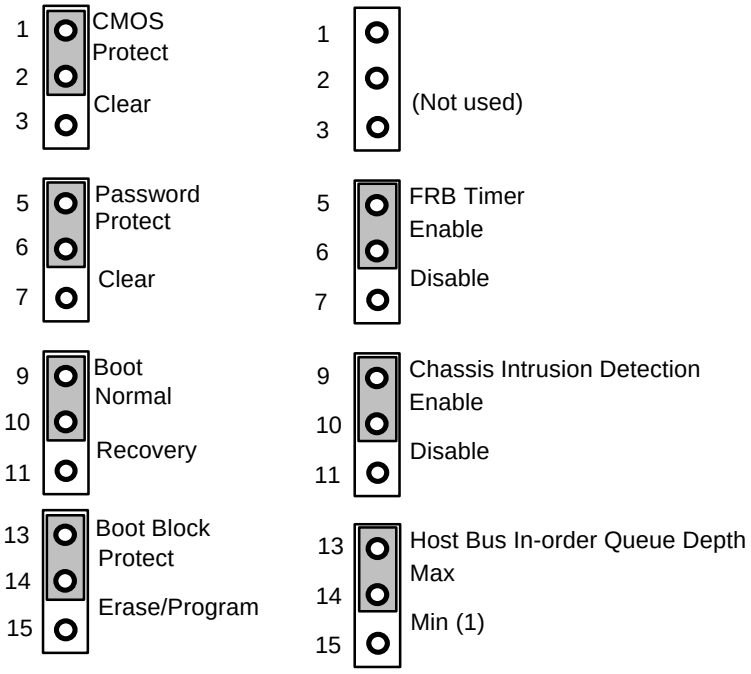

Figure 17 System Configuration Jumpers

The following table describes each jumperable option.

Table 22 System Configuration Jumper Options

Option	Description
CMOS Clear	If pins 1 and 2 are jumpered (default), NVRAM contents are preserved through system reset. If pins 2 and 3 are jumpered, NVRAM contents are set to manufacturing default during system reset.
Password Clear	If pins 5 and 6 are jumpered (default), the current system password is maintained during system reset. If pins 6 and 7 are jumpered, the password is cleared on reset.
Recovery Boot	If pins 9 and 10 are jumpered (default) the system will attempt to boot using the BIOS programmed in the Flash memory. If pins 10 and 11 are jumpered, the BIOS will attempt a recovery boot, loading BIOS code from a floppy disk into the Flash device. This is typically used when the BIOS code has been corrupted.
Boot Block Write Protect	If pins 13 and 14 are jumpered (default), the BIOS boot block is write-protected. If pins 14 and 15 are jumpered, the boot block is erasable and programmable. ***WARNING: Incorrect programming of the boot block will render the system unbootable.***
FRB Timer Enable	If pins 5 and 6 are jumpered (default) FRB operation is enabled, which allows the system to boot from processor 1 if processor 0 fails. If pins 6 and 7 are jumpered, FRB is disabled.
Chassis Intrusion Detection	If pins 9 and 10 are jumpered (default), a switch installed on the chassis will indicate when the cover has been removed. If pins 10 and 11 are jumpered, the chassis intrusion switch is bypassed.
Host bus In-order Queue	If pins 13 and 14 are jumpered (default), the host in-order queue depth is set at maximum. If pins 14 and 15 are jumpered, the depth is set at 1 (used for debugging purposes).

Speaker Circuit Jumper/Connector

A 4-pin single inline header provides a way to plug in an external speaker or, by jumper, a connection to the onboard speaker. The configuration is shown in the figure below.

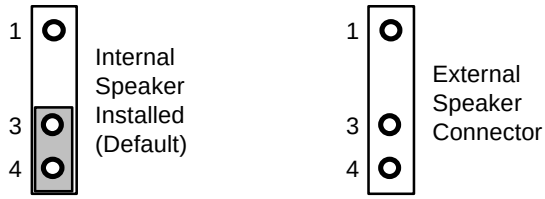

Figure 18 Speaker Circuit Jumper

Appendix D BIOS, Setup, SCU and SCSI Utility

BIOS Overview

The term “BIOS" refers to the following:

- System BIOS, that controls basic system functionality using stored configuration values.
- Configuration Utilities (CU) consisting of Flash ROM-resident Setup utility and system memory-resident System Configuration Utility (SCU), that provides user control of configuration values stored in NVRAM and battery-backed CMOS configuration RAM.
- Flash Memory Update utility (IFLASH), that loads predefined areas of Flash ROM with Setup, BIOS, and other code/data.

The following figure shows the relationship between BIOS components and register spaces. Unshaded areas are loaded into Flash using the Flash Memory Update Utility (IFLASH).

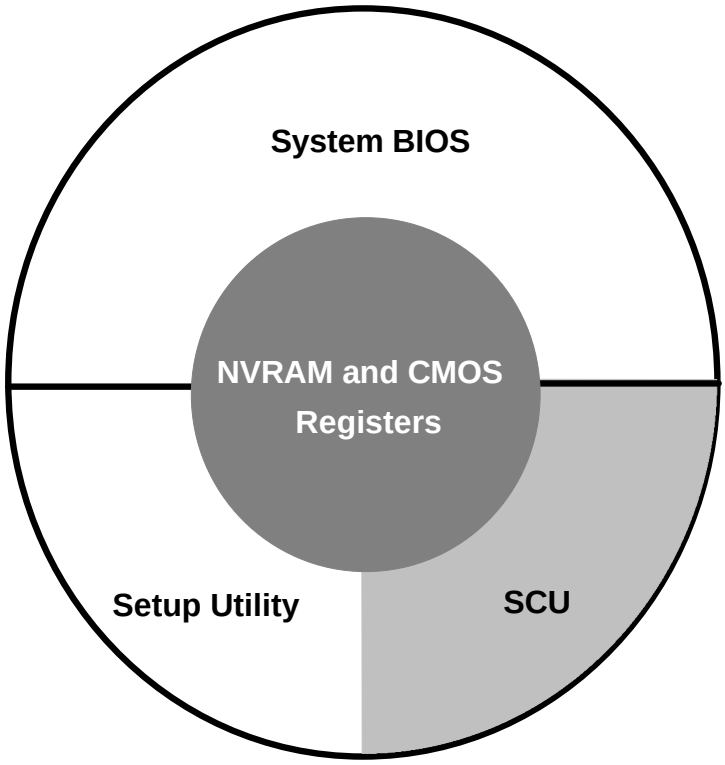

Figure 19 R440LX BIOS Architecture

System BIOS

The system BIOS is the core of the Flash ROM-resident portion of the BIOS. The system BIOS provides standard PC-BIOS services and some new industry standards, such as Plug and Play, DMI. In addition, the system BIOS provides support for these M440LX-specific features: security features, multiple-speed processor support, SMP support, fault resilient booting (FRB), logging of critical events, server management features, CMOS configuration RAM defaults, multiple language support, defective DIMM detection and remapping, automatic detection of video adapters, PCI BIOS interface, option ROM shadowing, system information reporting, ECC support, SMI support, user-supplied BIOS support, L2 cache support, I_2O support, memory sizing, boot drive sequencing, and resource allocation support.

The BIOS Setup and System Configuration Utility (SCU) are covered in detail in the M440LX Product Guide.

Appendix E Board Set Specifications

This chapter specifies the operational parameters and physical characteristics for R440LX DP Server. This is a board-level specification only. System specifications are beyond the scope of this document.

Absolute Maximum Ratings

Operation of R440LX at conditions beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only). Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 23 Absolute Maximum Conditions

Operating Temperature	0°C to +55°C *
Storage Temperature	-55°C to +150°C
Voltage on any signal with respect to ground	-0.3V to V_{DD} + 0.3V **
3.3V Supply Voltage with Respect to ground	-0.3 to +3.63V
5V Supply Voltage with Respect to ground	-0.3 to +5.5V

Chassis design must provide proper airflow to avoid exceeding Pentium Pro maximum case temperature.** V_{DD} means supply voltage for the device.

Further topics in this chapter specify normal operating conditions for R440LX.

Electrical Specifications

DC specifications for R440LX power connectors and module power budgets, are summarized here. Electrical characteristics for major connector interfaces (including DC and AC specifications), can be obtained from other documents:

- PCI Connectors -- *PCI Local Bus Specification Rev. 2.1*
- ISA slots -- *EISA Bus Specification*

Power Connection

Main power supply connection is obtained using the 24-pin main connector, which attaches to the power supply via 18 AWG wire of the color shown below.

Table 24 24-pin Main Power Connector Pinout

Pin	Signal	Color	Pin	Signal	Color
1	+5 Vdc	Red	13	+5 Vdc	Red
2	+5 Vdc	Red	14	+5 Vdc	Red
3	-5 Vdc	White	15	+5 Vdc	Red
4	-12Vdc	Blue	16	+5 Vdc	Red
5	COM	Black	17	COM	Black
6	COM	Black	18	COM	Black
7	COM	Black	19	COM	Black
8	COM	Black	20	COM	Black
9	COM	Black	21	COM	Black
10	+3.3 Vdc	Orange	22	+3.3 Vdc	Orange
11	+12 Vdc	Yellow	23	+3.3 Vdc	Orange
12	+12 Vdc	Yellow	24	+12 Vdc	Yellow

Mechanical Specifications

The following diagrams show the mechanical specifications of the Redwood baseboard. All dimensions are given in inches, and are dimensioned per ANSI Y15.4M. Maximum primary-side component height is .550” unless otherwise noted. Connectors are dimensioned to pin 1. Refer to “Connector Specifications” after the diagram for more information.

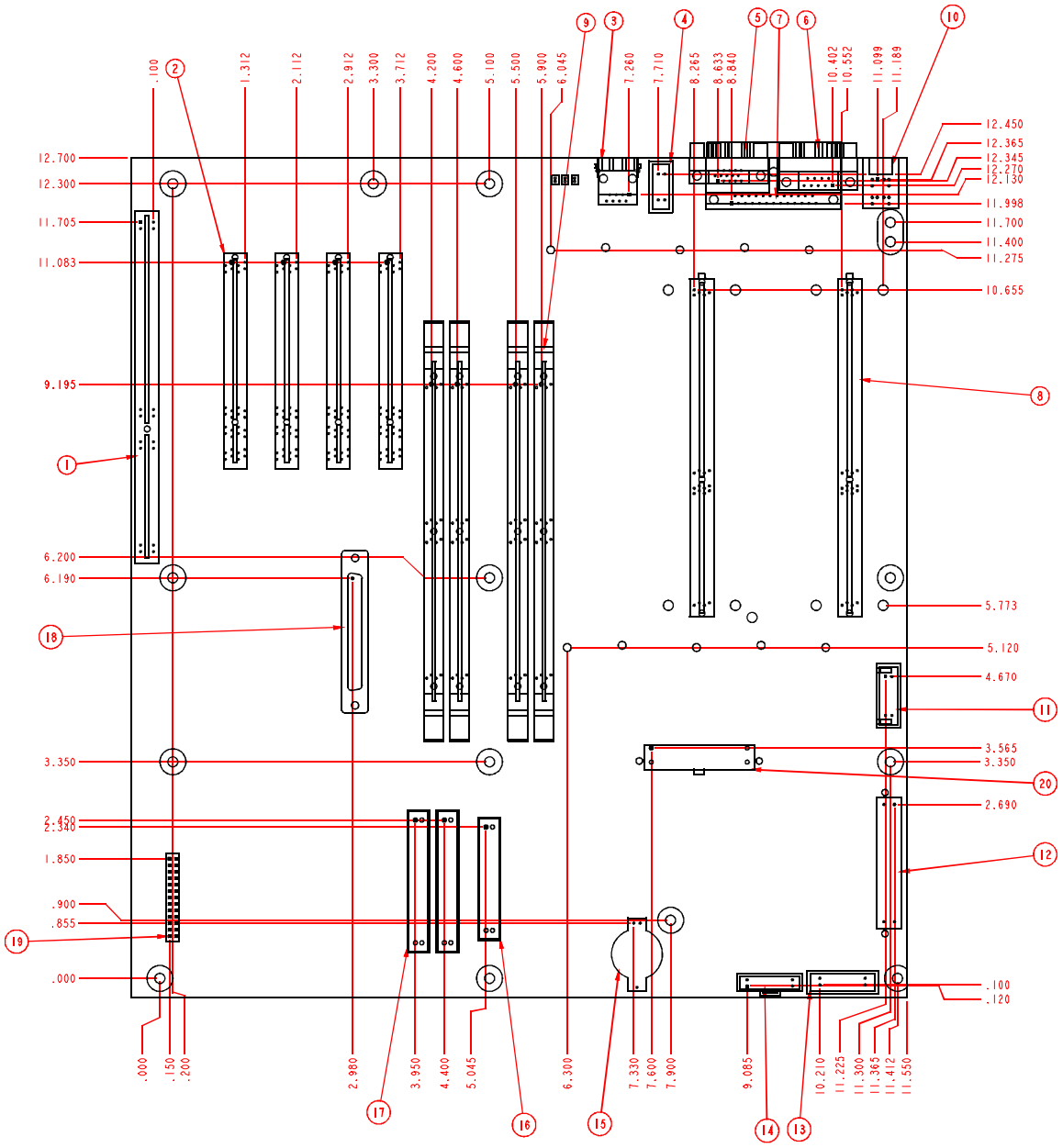

Figure 20 Baseboard Mechanical Diagram

Connector Specifications

The following table shows the quantity, and manufacturer's part numbers for connectors on the baseboard. Item numbers reference the circled numbers on the mechanical drawing. Refer to manufacturers' documentation for more information on connector mechanical specifications.

Table 25 Baseboard Connector Specifications

Item	Qty.	Mfr(s). and Part #	Description
1	1	AMP 176139-2	ISA bus add-in card connector
2	4	AMP 145154-4	PCI add-in card connector
3	1	AMP 555153-6	Ethernet connector
4	1	AMP 111950-1	Second Serial Port Header
5	1	Fox Conn/Hon Haj DZ11A36-R9	15-pin VGA connector
6	1	AMP 787650-4	9-pin Serial port D-sub connector
7	1	Fox Conn/Hon Haj DM11356-R1	25-pin Parallel port connector
8	2	AMP 145251-1 or -2	Slot 1 Processor Card Connector
9	4	Molex 71736-0008	Memory DIMM Connector
10	1	AMP 84376-1	Keyboard and mouse connector
11	1	AMP 111950-2	14-pin header, Columbus 2 Power Control
12	1	Molex 39-29-9242	24-pin power connector, Columbus 2 style
13	1	AMP 111950-3	Front panel connector
14	1	AMP 104068-3	ITP Connector (not installed)
15	1	Renata Batteries US HU 2032-1	Battery Holder
16	1	3M 2534-60V2UG	Floppy connector
17	2	Fox Conn/Hon Haj HL09207-D2	IDE connector
18	1	Fox Conn/Hon Haj QA01343-P4	68-pin SCSI connector
19	1	AMP 111970-6	Server Monitor Module feature connector
20	1	Molex 39-29-9202	20-pin power connector, ATX style
21	2	AMP 644486-3	3-pin System Fan Conn.
22	2	Fox Conn/Hon Haj HF08030-P1	3-pin Fan Sink Connector

PCI and ISA Connectors

The baseboard PCI and ISA connectors adhere to the requirements in the *PCI Local Bus Specification* and *ISA Specification*. Refer to these documents for connector specifications.

Processor Card Connectors

Refer to the *Pentium® II Processor EMTS* for connector specifications.

Appendix A. Supported Environments

The R440LX UP Server has been validated with the leading network operating systems,

Validated Operating Systems

- Level 1 - Heavy testing done in Intel's Server Validation Lab
- Level 2 - Minimal testing done in one of Intel's compatibility labs

Table 26 Validated Operating Systems

Level	Operating System	Version	Certified
1	Windows NT	Versions 4.0	OEM must certify w/Microsoft
1	Novell NetWare	4.11 SMP	Scheduled
2	MS DOS	6.22	N/A
1, 2	SCO UNIX	Unixware 2.1.1	OEM must certify W/SCO

Appendix B. Product Codes/Spares

Product Codes

Table 27 R440LX Baseboard Codes

Description	Product code
Baseboard, no retention, no termination card	B2RD265X32PP
Base board without retention mech, without term card	B0RD0STD
Baseboard with retention and term card	BOXR440LX

Table 28 R440LX DP Server System Codes

Description	Product code
System with 2 266MHz Proc, 32MB memory, 16x CD-ROM, with term card, with retention	S2RDCL265X32PP
System with 0 CPU, 0 memory, No CD-ROM, No term card, with retention	S0RDCL0X0XSD
System with 1 266mhZ CPU, 0 memory, No CD-ROM, with term card, with retention	S1RDCL265X0XSD
System with 1 266mhZ CPU, 0 memory, 16x CD-ROM, with term card, with retention	S1RDCL265X0CSD
System with 1 233mhZ CPU, 0 memory, No CD-ROM, with term card, with retention	S1RDCL235X0XSD

The R440LX project consists of a baseboard product and one system product. The table below characterizes the specifics of the baseboard and system products.

Table 29 System Product Details

PRODUCT CODE	PROCESSOR	MEMORY	Term. Card	Retention module	EXTERNAL DRIVE	INTERNAL DRIVE
S2RDCL265X32PP	Dual 266MHz 512 ECC Pentium II processor	1-32MB SDRAM DIMM	YES	NO	1-IDE CDROM (Hitachi 16X)	1 1GB IDE drive
S0RDCL0X0XSD	None	None	YES	YES	None	None
S1RDCL265X0XSD	Single 266MHz 512 ECC Pentium II processor	None	YES	YES	None	None
S1RDCL265X0CSD	Single 266MHz 512 ECC Pentium II	None	YES	YES	1-IDE CDROM	None

	processor				(Hitachi 16X)	
S1RDCL235X0XSD	Single 233MHz 512 ECC Pentium II processor	None	YES	YES	None	None

PP - Pre-Production, SD - Production

Spares

Table 30 Spares list

CPU retention mechanism	FRU660391
Country Kit	FRU684548
Chassis Assy	FRU651331
Fan, 120MM	FRU621116
SLT1 TERM Terminator Bd	FRU660391
Cable, Floppy	FRU654277
275W Power supply	FRU661386
Integrators kit	ACOLINTKIT

Appendix C. Connector Pin-outs

PCI Connectors

The following table defines the pin-out for each PCI expansion connector on the R440FX UP Server. Signals which are unused are labeled as either “Reserved”, or by signal mnemonic with the R440FX UP Server implementation shown in parentheses.

Table 31PCI Connector Signal Pin-out

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	-12V	A32	AD17	B1	TRST_L (p/d)	B32	AD16
A2	TCK (p/d)	A33	C/BE2_L	B2	+12V	B33	+3.3V *
A3	GND	A34	GND	B3	TMS (p/u)	B34	FRAME_L
A4	TDO (n/c)	A35	IRDY_L	B4	TDI (p/u)	B35	GND
A5	+5V	A36	+3.3V *	B5	+5V	B36	TRDY_L
A6	+5V	A37	DEVSEL_L	B6	INTA_L	B37	GND
A7	INTB_L	A38	GND	B7	INTC_L	B38	STOP_L
A8	INTD_L	A39	LOCK_L	B8	+5V	B39	+3.3V *
A9	PRSNT1_L	A40	PERR_L	B9	Reserved	B40	SDONE (p/u)
A10	Reserved	A41	+3.3V *	B10	+5V	B41	SBO_L (p/u)
A11	PRSNT2_L	A42	SERR_L	B11	Reserved	B42	GND
A12	GND	A43	+3.3V *	B12	GND	B43	PAR
A13	GND	A44	C/BE1_L	B13	GND	B44	AD15
A14	Reserved	A45	AD14	B14	Reserved	B45	+3.3V *
A15	GND	A46	GND	B15	RST_L	B46	AD13
A16	CLK	A47	AD12	B16	+5V	B47	AD11
A17	GND	A48	AD10	B17	GNT_L	B48	GND
A18	REQ_L	A49	GND	B18	GND	B49	AD9
A19	+5V	A50	key	B19	Reserved	B50	key
A20	AD31	A51	key	B20	AD30	B51	key
A21	AD29	A52	AD8	B21	+3.3V *	B52	C/BE0_L
A22	GND	A53	AD7	B22	AD28	B53	+3.3V *
A23	AD27	A54	+3.3V *	B23	AD26	B54	AD6
A24	AD25	A55	AD5	B24	GND	B55	AD4
A25	+3.3V *	A56	AD3	B25	AD24	B56	GND
A26	C/BE3_L	A57	GND	B26	IDSEL	B57	AD2
A27	AD23	A58	AD1	B27	+3.3V *	B58	AD0
A28	GND	A59	+5V	B28	AD22	B59	+5V
A29	AD21	A60	ACK64_L (p/u)	B29	AD20	B60	REQ64_L (p/u)
A30	AD19	A61	+5V	B30	GND	B61	+5V
A31	+3.3V *	A62	+5V	B31	AD18	B62	+5V

* 3.3V system power is not present at this pin..

NOTE: The R440LX DP Server does not provide a PCI 3.3V power connector. Only the 5V PCI signaling environment is supported, and no power is available at the 3.3V signal pins in expansion slots.

ISA Connectors

Table 32 ISA Connector Signal Pin-out

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A01	IOCHK_L	A26	SA5	B01	GND	B26	DACK2_L
A02	SD7	A27	SA4	B02	RESDRV	B27	TC
A03	SD6	A28	SA3	B03	+5V	B28	BALE
A04	SD5	A29	SA2	B04	IRQ9	B29	+5V
A05	SD4	A30	SA1	B05	-5V	B30	OSC
A06	SD3	A31	SA0	B06	DRQ2	B31	GND
A07	SD2	C01	SBHE_L	B07	-12V	D01	MEMCS16_L
A08	SD1	C02	LA23	B08	NOWS_L	D02	IOCS16_L
A09	SD0	C03	LA22	B09	+12V	D03	IRQ10
A10	IOCHRDY	C04	LA21	B10	GND	D04	IRQ11
A11	AEN	C05	LA20	B11	SMWTC_L	D05	IRQ12
A12	SA19	C06	LA19	B12	SMRDC_L	D06	IRQ15
A13	SA18	C07	LA18	B13	IOWC_L	D07	IRQ14
A14	SA17	C08	LA17	B14	IORC_L	D08	DACK0_L
A15	SA16	C09	MRDC_L	B15	DACK3_L	D09	DRQ0
A16	SA15	C10	MWTC_L	B16	DRQ3	D10	DACK5_L
A17	SA14	C11	SD8	B17	DACK1_L	D11	DRQ5
A18	SA13	C12	SD9	B18	DRQ1	D12	DACK6_L
A19	SA12	C13	SD10	B19	REFRESH_L	D13	DRQ6
A20	SA11	C14	SD11	B20	BCLK	D14	DACK7_L
A21	SA10	C15	SD12	B21	IRQ7	D15	DRQ7
A22	SA9	C16	SD13	B22	IRQ6	D16	+5V
A23	SA8	C17	SD14	B23	IRQ5	D17	MASTER16_L
A24	SA7	C18	SD15	B24	IRQ4	D18	GND
A25	SA6	--	--	B25	IRQ3	--	--

Serial Port Connectors

Table 33 Serial Port Connector Pin-out

Pin	Name	Description
1	DCD	Data Carrier Detected
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Ground
6	DSR	Data Set Ready
7	RTS	Return to Send
8	CTS	Clear to Send
9	RIA	Ring Indication Active

Serial Port B

The pin-out below shows pin-outs from serial port B from the board-level perspective. Note that the system uses a short cable to connect from the board to the serial port on the chassis, and that this cable makes serial port B have the same pin-out as serial port A.

Table 34 Serial Port B

Pin	Name	Pin	Name
1	DCD	6	CTS
2	DSR	7	DTR
3	RXD	8	RI
4	RTS	9	GND
5	TXD	10	key

Parallel Port Connector

Table 35 Parallel Port Connector Pin-out

Pin	Name	Pin	Name
1	STROBE_L	14	AUFDXT_L
2	D0	15	ERROR_L
3	D1	16	INIT_L
4	D2	17	SLCTIN_L
5	D3	18	GND
6	D4	19	GND
7	D5	20	GND
8	D6	21	GND
9	D7	22	GND
10	ACK_L	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT		

Keyboard and Mouse Connectors

The keyboard and mouse connectors are mounted within a single housing. Although functionally equivalent, the mouse connector is defined as the one above the keyboard connector.

Table 36 Mouse Connector Pin-out

Pin	Signal	Description
7	MSEDAT	Mouse Data
8	(NC)	
9	GND	
10	FUSED_VCC	
11	MSECLK	Mouse Clock
12	(NC)	

Table 37 Keyboard Connector Pin-out

Pin	Signal	Description
1	KEYDAT	Keyboard Data
2	(NC)	
3	GND	
4	FUSED_VCC	
5	KEYCLK	Keyboard Clock
6	(NC)	

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