SPECIFICATION

echnology for **MMX**™ CPUs (including
M2, and AMD K6)

33/166/180/200/233 MHz Pentium™
cket

and P55C

, IBM 6x86, and AMD K5/K6 CPUs

ge Mode SIMM modules auto banking in
to 256MB

M to support SDRAM/EDO DRAM/Page Mode DRAM

nfiguration so that DIMM and SIMM can be installed in any
SIMM 1, 2 and DIMM 2 can not be installed at the same time

system memory through SIMM and DIMM Sockets

Pipelined Burst synchronous cache

and three 16 bits ISA Bus slots

Master Mode

ur IDE hard disk drives without device driver for *S/W*
ty of each hard disk can be larger than 528MB up to 8.4GB

IDE interface with two connectors supports four IDE devices in
DE Controller supports PIO Mode 0 to Mode 4 at maximum
s and Bus Master IDE DMA Mode 2

chip that supports two serial ports with 16550 Fast UART
ort with EPP and ECP capabilities, and one floppy disk drive

rial Bus (USB)

CR810 SCSI BIOS firmware and Green feature function

M .

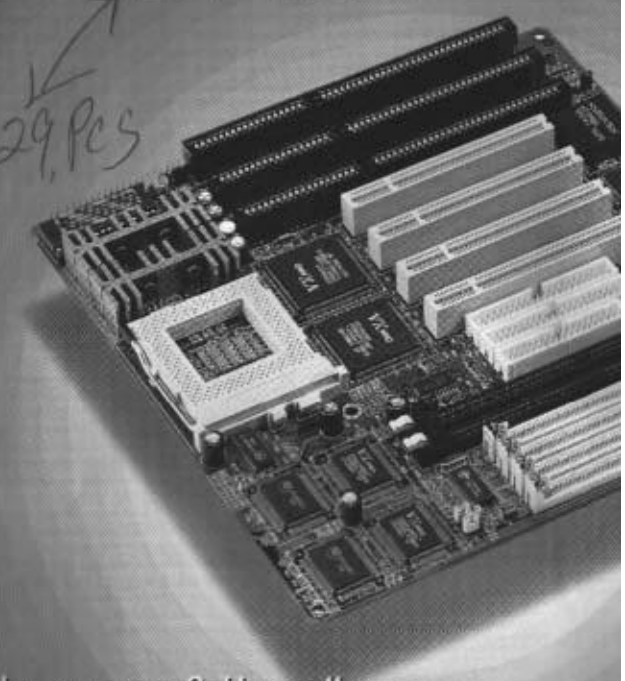
CE

586 Mainb

New Generation VXPRO Chip
PCI Bus and ISA Bus

7504-1B0

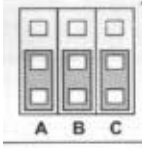
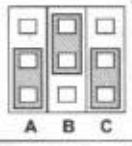
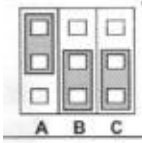
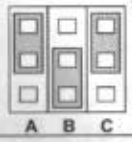
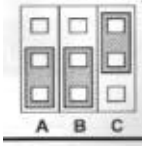
29 PCS



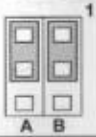
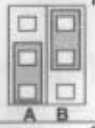
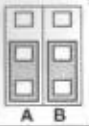
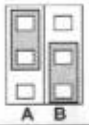
INTRODUCTION & USER'S MANUAL

- With PCI IDE & Multi I/O
- Fully Compatible with Intel MMX™ Techn
- VXPRO Chipset
- Features SDRAM Modules
- Offers High Degree of Flexibility with Revo
- Combined DIMM and SIMM Configuratio

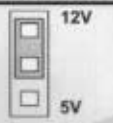
ed Jumpers

JP3A~C	CPU Clock	JP3A~C
	66MHz	
	75MHz	
		

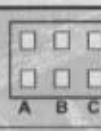
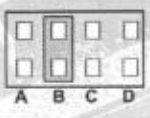
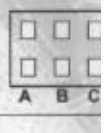
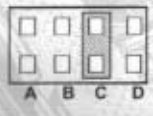
rnal Clock Speed Jumpers

rix	AMD	JP5
served	1.5X	
)X	Reserved	
served	2.5X	
served	3.0X	

JP4: Flash ROM Voltage Jumper

Description	JP4
12 Volt Flash programming	
5 Volt Flash programming	

JP6-A, B, C, D:CPU Voltage Regulato

	Setting		Setti
3.5V		2.7V	
2.9V		2.5V	
2.8V			

PS1: PS/2 Mouse Connector

Pin	Description
1	Mouse Data
2	N.C.
3	Ground
4	+5V
5	Mouse CLK
6	N.C.

USB
Univ
Bus

Pin
1,2
3,4
5,6
7,8
9,1

ck Installation Guide

RAM discharge jumper (pin 1 - 2)

PU speed

PU Internal Clock Speed

) to select CPU Voltage Regulator Output

socket

M modules into SIMM1 - 4 and/or insert 168-pin
o DIM1 - 2, notice that DIM2 and SIMM1,2
at the same time

nto system chassis

to J1

ard and other peripheral cards (if required) onto

s) to IDE primary/secondary connector(s)

ve(s) to FDC1 connector

s to COM1 and COM2 connectors

rt to PRN1 connector

LED to "Hard Disk Busy" LED on the system

D to Turbo LED on the system chassis

Reset Switch on the system chassis

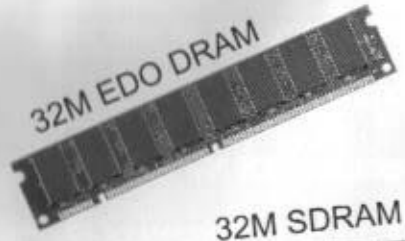
Speaker on the system chassis

OCK to keylock and power LED on the system

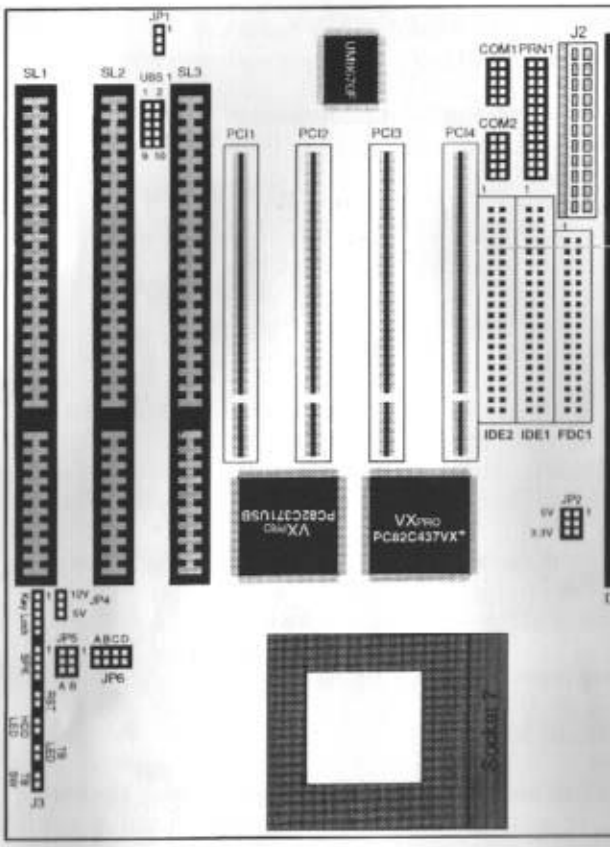
d to
onnector

is,

puter.



Jumper Setting



J1 Keyboard Connector

A standard five-pin female DIN k
located at the rear of the board J1

Pin	Description
1	Keyboard Clock
2	Keyboard Data
3	N.C.
4	Ground
5	+5VDC

Jumper Settings

upply Connector

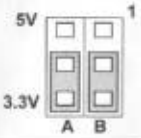
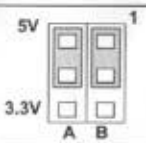
scription	Pin	Description
wer Good	7	Ground
VDC	8	Ground
2VDC	9	- 5VDC
2VDC	10	+5VDC
ound	11	+5VDC
ound	12	+5VDC

AM Discharge Jumper

scription
ernal Battery sitive
nnector to OS
ound

Description	JP1
Internal Battery Mode	
Discharge CMOS	

odule Voltage Selector

ion	JP2
AM DIMM 3.3V)	
DRAM / Fast AM DIMM 5V)	

Jumper Settin

J3: RST (Reset Switch Conn

Setting	Description
Open	Normal Mode
Short	Reset System

J3: KEYLOCK(Keylock & Power LED Connector)

Pin	Description
1	LED Output
2	N.C.
3	Ground
4	Keylock
5	Ground

J3: TE Co

Pi
1
2

J3 SPK (Speaker Connector) J3

Pin	Description
1	DATA Out
2	N.C.
3	Ground
4	+5V