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TMC

User's Manual
PCI54PV Motherboard
1st Edition

Contents

About This Manual

This manual is organized as follows:

Chapter I Introduction - Introduces the PCI54PV motherboard.

Chapter 2 Specifications - Lists and explains the specifications of the PCI54PV motherboard.

Chapter 3 Hardware Description - Describes each of the major features of the PCI54PV motherboard. Also describes the main memory configurations of the board.

Chapter 4 Configuring the PC154PV - Describes the necessary procedures and jumper settings to configure the PC154PV motherboard.

Chapter 5 Installation - Describes the interfaces and connectors. The PC154PV provides for creating a working system.

Chapter 1 Introduction

The PCI54PV is a high performance, P54C/CT microprocessor powered, ISA/VESA PCI Local Bus motherboard. The P54C/CT processor is designed for high-end desktop and server computers.

The PCI54PV contains a total of five ISA expansion slots and Four PCI slots. Two of these ISA slots have VESA Local(VL)-Bus connectors, allowing users to install VL-Bus peripheral cards such as a high resolution graphics card and a high performance storage controller. Two VL-Bus slots and Four PCI Bus slots of the PC154PV support bus mastering further enhancing system.

The P54C/CT processor includes separate code and data caches to provide high performance. Each cache is 8KB in size and the data cache can be configured to be write-through or write-back on a line by line basis. In addition to 16KB of on-chip cache memory, the PC154PV can be configured with up to 512KB of write-back secondary cache memory, further improving system performance.

The on board SIMM sockets are designed to accommodate 256K x 36, 1M x 36, or 4M x 36 modules as well as dual density modules including 512K x 36, 2M x 36 or 8M x 36, providing the user with up to 128GB of system memory.

The performance, speed and expendability of the PCI54PV make it the perfect choice for building a LAN server, a high-end workstation, or a multi-user system. *Note, remember this board was manufactured in the early 1990s. The 486 was very common, and the Pentium chips hadn't been on the market very long. This was one of the fastest processors out.*

Chapter 2 Specifications

Main Processor
Intel P54C/CT 75/90/100 MHz microprocessor.

Cache Memory
256KB or 512KB of write-back secondary cache memory

Main Memory
Up to *128MB of* on board main memory
Two memory banks
Four 36-bit SIMM sockets for 256K x 36, 1M x 36 or 4M x 36 modules
The SIMM sockets also support dual density modules:
512K x 36, *2M* x 36 or 8M x 36

BIOS
Licensed BIOS

Clock/Calendar
Battery Backed Real Time Clock(146818 compatible) and 128 bytes of CMOS RAM. On board rechargeable battery

DMA Channels
Seven DMA channels (8237 compatible)

Interrupts
Sixteen levels of hardware interrupts (dual 8259 compatible)

System Timer
Three channels of programmable system timer (8254 compatible)

Expansion
Four PCI-Bus slots: four master slots
Two VL-Bus slots: one master slots
Five ISA slots

Connectors
Connectors for: power supply, keyboard, reset switch, Power LED, keylock, speaker, turbo switch, turbo LED, external battery and hard disk access LED.

Form Factor
Baby AT size

Power Requirement(typical)
+5V @ 3.5 AMPs

Chipset
OPTi 82C596/82C597/82C822

Chapter 3 Hardware Description

This chapter briefly describes each of the major features of the PC154PV system board. The function block of the board is shown in *Figure 1.* The layout of the board is shown in *Figure 2* to show the locations of key components. The topics covered in this chapter are as follows:

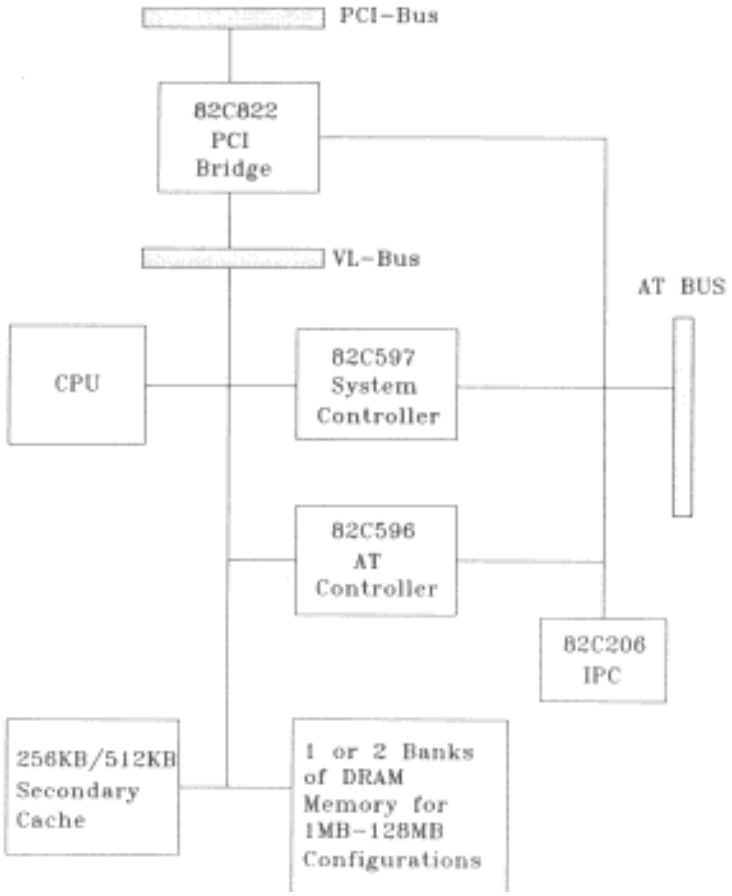


Figure 1: Function block of the PC154PV

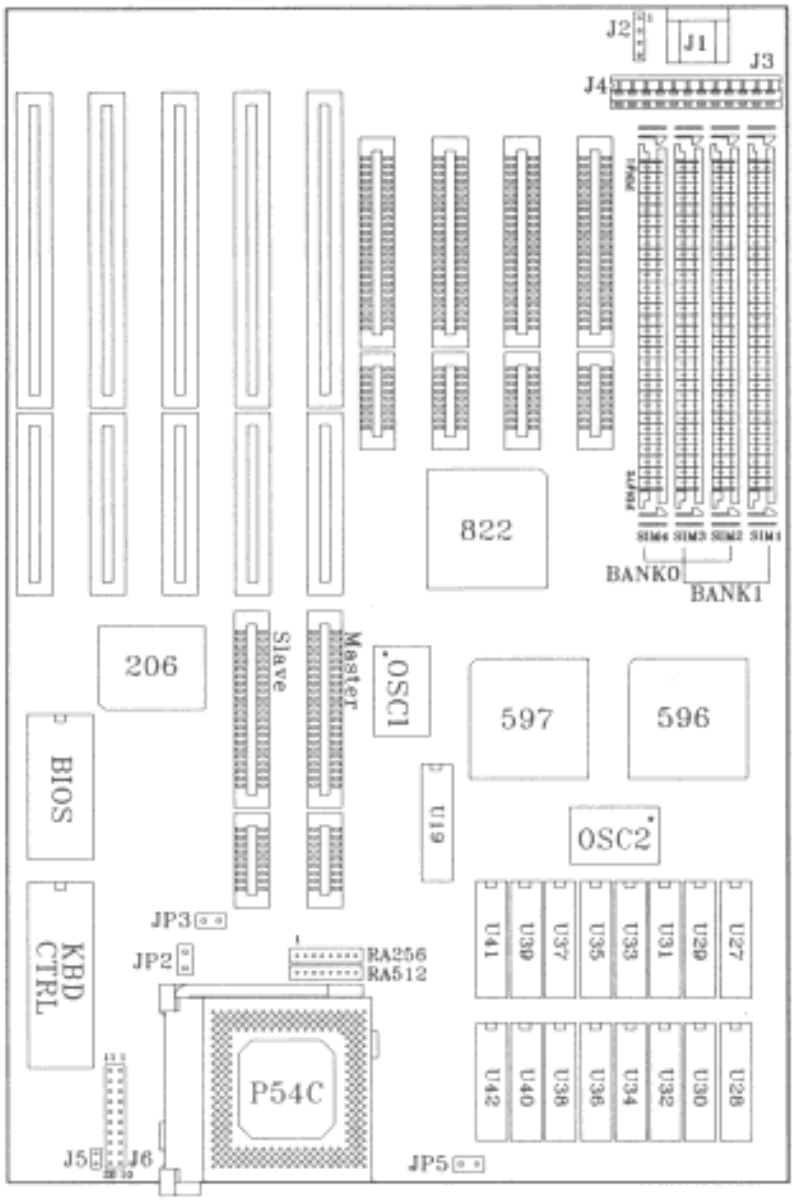


Figure 2: Layout and connector locations of the PC154PV

3.1 PCI54PV System Board

The PCI54PV is designed by implementing a P54C/CT microprocessor and a highly integrated chipset.

The 82C596 ATC (AT Controller) integrates the AT bus interface and the data buffers for transfers between the CPU data bus, Local data bus and the DRAM data bus. It also provides ISA to local bus command translation.

The 82C206 Integrated Peripherals Controller (IPQ incorporates the DMA Controller, Interrupt Controller, System Timer, and Clock/Calendar functions.

The chipset is comprised of three chips, the 82C597 SYSC controller 82C596 ATC controller and 82C822 PCIB controller (VESA Bus to PCI Bridge chip). The SYSC (System Controller) provides the control functions for the host CPU interface, the 32-bit local bus interface, the 64-bit secondary cache memory and 64-bit DRAM bus. The SYSC controls the data flow between the CPU bus, the DRAM bus, the local bus, and the 16/8-by ISA bus. The PCIB provides all of the control, Address and Data paths to implement the PCI Bus from a VESA VIL-Bus.

3.2 P54C/CT Microprocessor

The P54C/CT processor is designed for high performance desktops and servers and is binary compatible with both the 486DX and 386DX.

The application instruction set of the P54C/CT processor includes the complete 486 CPU instruction set with extensions to accommodate some of the additional functionality of the P54C/CT processor. All application software written for the 386 and 486 microprocessors will run on the P54C/CT processor without modification.

The P54C/CT implements several enhancements to increase performance. The P54C/CT processor has increased the data bus to 64-bits and contains separate code and data cache of 8KB each with a cache line size of 32-bytes. The P54C/CT processor also contains a pipelined floating-point unit that provides a significant floating-point performance advantage over previous generations of the P54C/CT processor.

3.3 Cache Memory

The P54C/CT processor includes separate code and data caches integrated on chip to provide high performance. Each cache is 8KB in size, with 32-byte line size and is 2-way set associative. The data cache is configurable to be write-back or write-through on a line by line basis.

For the secondary cache, the PC154PV supports write-back cache memory sizes of 256KB or 512KB.

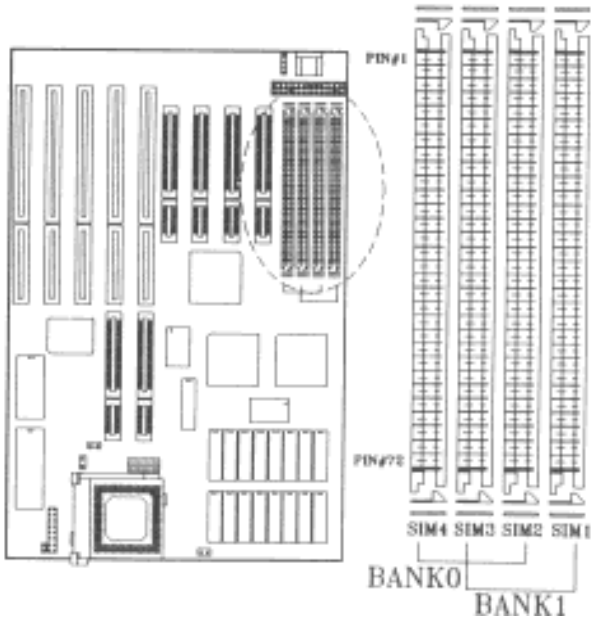
3.4 Main Memory

The PCI54PV has two (2) memory banks for up to *128MB* of main memory. Each memory bank of the PCI54PV consists of two (2) 36-bit SIMM (Single In-Line Memory Module) sockets that can accept *256K x 36, 1M x 36 or 4M x 36* modules.

The SIMM sockets can also accommodate dual density modules such as *512K x 36, 2M x 36 or 4M x 36* SIMMs.

Refer to the following figure for the locations of the PC154PV's memory banks.

Figure 3: **Memory bank locations of the PC154PV**



Total Memory	Bank 0	Bank 1
2MB	256K x 36	----
4MB	512K x 36	----
6MB	256K x 36	512K x 36
8MB	1M x 36	----
8MB	512K x 36	512K x 36
10MB	256K x 36	1M x 36
12MB	512K x 36	1M x 36
16MB	1M x 36	1M x 36
16MB	2M x 36	----
18MB	256K x 36	2M x 36
20MB	512K x 36	2M x 36
24MB	1M x 36	2M x 36
32MB	4M x 36	----
32MB	2M x 36	2M x 36
34MB	256K x 36	4M x 36
36MB	512K x 36	4M x 36
40MB	1M x 36	4M x 36
48MB	2M x 36	4M x 36
64Mb	8M x 36	4M x 36
64MB	4M x 36	----
66MB	256K x 36	8M x 36
68MB	512K x 36	8M x 36
72MB	1M x 36	8M x 36
80MB	2M x 36	8M x 36
96MB	4M x 36	8M x 36
128MB	8M x 36	8M x 36

Table 1: Memory configurations of the PCI54PV

3.5 BIOS

The PC154PV contains a 128Kx8 Flash ROM that contains the system BIOS. The BIOS resides at the upper 64KB of address space in the first megabyte.

In protected mode, the BIOS is also mapped to the upper 64KB of the 128NM space and can be accessed at either location.

The BIOS on the PC154PV is compatible with the BIOS in the IBM AT with the exception that it does not contain the BASIC interpreter. The BASIC and BASICA on IBM PCDOS will not run on the PC154PV.

To run BASIC in systems based on the PC154PV, the user should use the GW-BASIC interpreter provided with the Microsoft DOS diskette.

3.6 1/0 Port Address Map

The CPU of the PC154PV communicates via 1/0 ports. There is a total of 1K port address space defined. The following tables list the 1/0 port addresses used in the PC154PV and those assigned to other devices that can be used by the add-on cards.

Table 2: 1/0 port addresses of the devices on the PCI54PV

Address	Device Description
000h – 01Fh	DMA Controller #1
020h – 03Fh	Interrupt Controller #1
040h – 05Fh	Timer
060h – 06Fh	Keyboard Controller
070h – 07Fh	Real Time Clock, NMI
080h – 09Fh	DMA Page Register
0A0h – 0BFh	Interrupt Controller #2
0C0h – 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor

Table 3: 1/0 port addresses of devices on the 1/0 slots

Address	Description
1F0h – 1F7h	Primary IDE Interface
200h – 207h	Game Port
278h – 27Fh	Parallel Port #2 (LPT2)
300h – 31Fh	Prototype Card
360h – 36Fh	Reserved
378h – 3FFh	Parallel Port #1 (LPT1)
380h – 38Fh	SDLC #2
3A0h – 3AFh	SDLC #1
3B0h – 3BFh	MDA Video Card (Including LPT0)
3C0h – 3CFh	Reserved
3D0h – 3DFh	CGA Video Card
3F0h – 3F7h	Floppy Disk Controller
3F8h – 3FFh	Serial Port #1 (COM1)

3.7 Memory Map

The PC154PV has a maximum memory capacity of 128MB. The first megabyte is divided into four blocks with each block dedicated to a fixed function. The following table illustrates the memory map for the PC154PV.

Table 4: Memory map of the PCI54PV

Memory	Address	Description
0KB	000000h 09FFFFh	Conventional RAM
640KB	0A0000h 0BFFFFh	128KB of Video RAM
768KB	0C0000h 0EFFFFh	192KB of I/O Expansion ROM
960KB	0F0000h 0FFFFFh	64KB of System BIOS ROM
1MB	100000h 7FEFFFFh	127MB of User RAM
128MB	7FF0000h 7FFFFFFh	Duplicated 64KB of System BIOS ROM at 0F0000h

3.8 System Timer

The PC154PV has three channels of timer/counter in the 82C206 chip, which is Intel 8254 compatible. The function of each channel is listed as follows:

Table 5: System timer of the PCI54PV

Channel	Function
0	System Timer – This timer generates the time base for the system timer. Its output is tied to IRQ0.
1	Memory Refresh Request – This timer is used to generate memory refresh requests. It triggers the memory refresh cycle.
2	Tone Generator for Speaker – This timer provides the speaker tone. Various sounds can be generated by programming the timer.

3.9 DMA Channels

The PC154PV contains the equivalent of two 8237A DMA controllers in the 82C206.

The 82C206 provides the user with two DMA controllers, four channels of DMA(DMA # 1) for 8-bit transfers, and three channels of DMA(DMA #2) for 16 bit transfers. (The first 16-bit DMA channel is used for cascading.)

3.10 Interrupt Controllers

The PC154PV contains two Intel 8259A compatible interrupt controllers in the 82C206. Sixteen channels are partitioned into the cascaded controllers (INTCI1, INTC2) with 8 inputs each. Of these 16 channels, three are connected internally to various devices, allowing 13 user definable channels of interrupt. Any or all of these interrupts can be masked.

Channel Controller #1	Channel Controller #2	Function
0		DRQ0, Spare
1		DRQ1, Spare
2		DRQ2, Floppy Disk Controller
3		DRQ3, Spare
	4	DRQ4, Cascade for DMA
	5	DRQ5, Spare
	6	DRQ6, Spare
	7	DRQ7, Spare

Level	Function
NMI	RAM Parity Check
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ8	Real Time Clock
IRQ9	Software Redirected to Int 0Ah
IRQ10	Reserved
IRQ11	Reserved
IRQ12	Reserved
IRQ13	80287
IRQ14	Fixed Disk Controller
IRQ15	Reserved
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Parallel Port #2
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1

3.11 Real Time Clock and CMOS RAM

The PC154PV contains an MCI 46818 compatible Real Time Clock (RTC) and 128 bytes of CMOS RAM in the 82C206.

The CMOS RAM stores the system's configuration information entered via the Setup program. The RTC and the CMOS RAM are kept active by a battery when the system power is turned off.

Note: The Real Time Clock and the CMOS RAM are kept active by an on board rechargeable battery. The PCI54PV also provides an interface for an external battery. Refer to Section 5.2, "External Battery Connector", for details.

Chapter 4 Configuring the PC154PV

The following sections describe the necessary procedures and proper jumper settings to configure the PC154PV system board. For the locations of the jumpers and Resistor Arrays, refer to Figure 2 on page 3 - 2.

The following configuration options can be selected:

4.1 VL-Bus Write Wait State Jumper: JP5

4.2 Video Adapter Selection Jumper: JP2

4.3 Back to Back I/O Delay Selection: JP3

4.4 Secondary Cache Memory Size: RA256, RA512

4.1 VL-Bus Wait State Selection Jumper: JP5

This 2-pin header, JP5, determines whether or not an additional local bus clock cycle is necessary to perform a write to a VL-Bus peripheral device. Read cycles are unaffected by this setting.

Refer to the following table for the necessary settings.

Table 6: VL-Bus write wait state selection settings

JP5	Condition
	0 wait state writes *(default)*
	1 wait state writes

My experience with this is that if you use a VL Local bus card, this jumper must be set else the card won't work. (IE video or hard drive controller card).

4.2 Video Adapter Selection Jumper: JP2

This Jumper setting is checked by the system BIOS during system BIOS during system boot-up to decide what type of video card is primary card in the system board. This jumper setting is also checked against the configuration information stored in the CMOS RAM by the Setup program.

If there is only one video card installed in the PC154PV system, set this jumper to reflect its type.

If more than one video card is installed in the PC154PV system, set this jumper to indicate which card is the primary one.

Note:
If this jumper is set to indicate the type of primary display present in the PCI54PV, an error message will appear during boot-up. Also, note that for a videoless application, such as a dedicated file server, it is not necessary to set JP2. You may specify videoless application during the system setup program.

4.3 Back-to-Back I/O Delay Selection: JP3

This 2-pin header must be set according to the following table:

JP3	Function
	Enable back-to-back I/O delay *(default)*
	Disable back-to-back I/O delay

4.4 Secondary Cache Memory Size Selection Resistor Arrays: RA256, RA512

These two (2) 8-pin RA (Resistor Array) sockets **(RA256 and RA512)** allow the user to indicate the amount of secondary cache memory present on the PCI54PV.

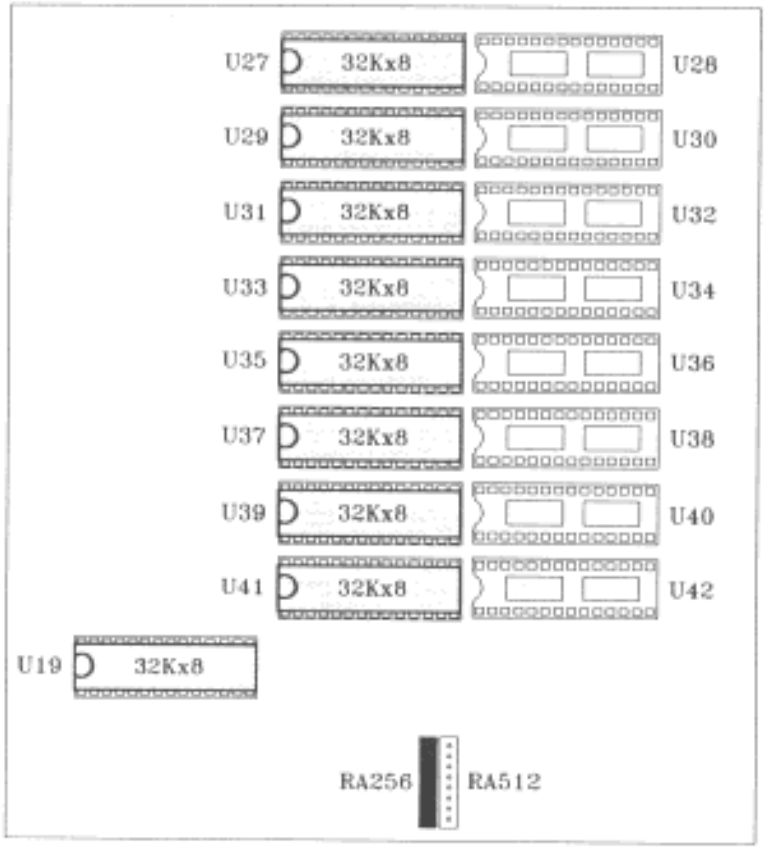
The secondary cache RAM improves the system performance by providing the P54C/CT CPU with data in the event of on-chip cache misses. The secondary cache RAM of the PCI54PV implements the write-back design, further improving system performance.

The PCI54PV supports two cache memory sizes: *256KB or 512KB.* Refer to the following pages for the necessary procedures on installing or changing the cache memory size of the PCI54PV.

Note
Depending on the user's specified cache memory size, these RAs(RA256, RA512) will be preconfigured by the manufacturer. Therefore, unless the user changes the cache size of the PCI54PV, reconfiguration of these RNs WILL NOT be necessary.

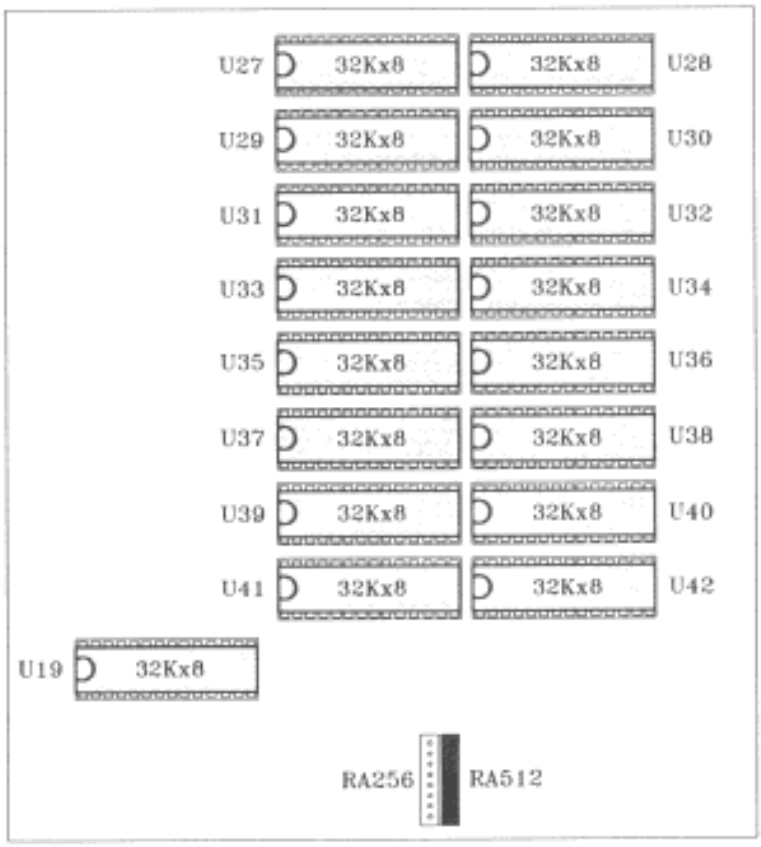
To configure the PCI54PV with 256KB of secondary cache memory, install eight(8) 32K x 8 SRAM in sockets U27, U29, U31, U33, U35, U37, U39 and U41 for the cache data RAM and one (1) 32K x 8 SRAM in U19 for the tag RAM.

Also, Install the RAs in RA256. Refer to the following figure for the locations of the SRAM and the Resistor Arrays.


U27
32Kx8
U28
U29
32Kx8
U30
U31
32Kx8
U32
U33
32Kx8
U34
U35
32Kx8
U36
U37
32Kx8
U38
U39
32Kx8
U40
U41
32Kx8
U42
U19
32Kx8
RA256
RA512

512KB of secondary cache memory is achieved by installing sixteen (16) *32K x 8* SRAM in U27 - U42 for the cache data RAM and one (1) *32K x 8* SRAM in U19 for the tag RAM.

Also, install the RAs in RA512. Refer to the following figure for the locations of the SRAM and the RAs.



Chapter 5 Installation

This chapter describes the interface that the PCI54PV provides for creating a working system. Refer to Figure 2 for the location of the connectors.

The following items are covered in this chapter:

5.1 External Battery Connector: J2
5.2 Keyboard Connector: J1
5.3 Power Supply Connectors: J3 & J4
5.4 Speaker Connector: J6 (Pins 1-4)
5.5 Power LED and Keylock Connector: J6 (Pins 11 - 15)
5.6 Turbo LED connector: J6 (Pins 8 & 18)
5.7 Reset Switch Connector: J6 (Pins 9 & 19)
5.8 Hard Disk Access LED Connector J6 (Pins 10 & 20)
5.9 Installing a P54C/CT Processor
5.10 Battery Selection: JP1
5.11 LDEV# Sample Selection: JP4
5.12 VL Bus wait state selection jumper: JP5

5.1 External Battery Connector: J2

This 4-pin connector, J2, allows the user to connect an external battery to maintain the information stored in the CMOS RAM.

J2 Pin #	Description
1	Vcc
2	N. C.
3	Ground
4	Ground

5.2 Keyboard Connector: J1

The keyboard connector, J1, is a 5-pin DIN connector for attaching an IBM AT or an IBM Enhanced 101-key compatible keyboard.

The following describes the pin-out assignment of this connector:

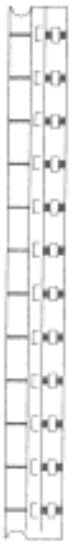
J1 Pin #	Function
1	Keyboard Clock
2	Keyboard Data
3	N.C.
4	Ground
5	V_{cc}

5.3 Power Supply Connectors: J3 and J4

When using an AT compatible power supply, plug both of the power supply connectors into J3 and J4.

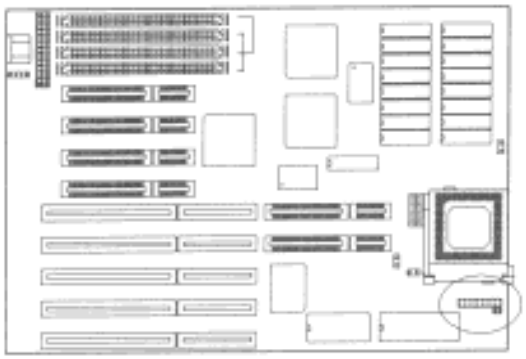
Make sure the power supply connectors are connected in the right orientation. The power supply connectors are connected in the right orientation if the black wires of each power cable are ADJACENT to each other. That is, black wires of each connector should be aligned in the center of the power supply connectors, J3 and J4 of the PCI54PV.

The following table indicates the pin-out assignments of the power supply connectors.

Pin #		Description	Wire Color
1		Power Good	Orange
2		+ 5 V	Red
3		+ 12 V	Yellow
4		- 12 V	Blue
5		Ground	Black
6		Ground	Black
7		Ground	Black
8		Ground	Black
9		- 5 V	White
10		+ 5 V	Red
11		+5 V	Red
12		+5 V	Red

J6 pinouts:

J6 is a connector that supplies many different components. This table is a tabulation of all the pins. See the separate descriptions for related groupings. The circled jumper below is J6.

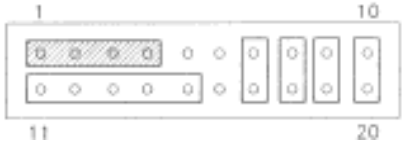


J6 Pin #	Function
1	Speaker Out
2	N. C.
3	Ground
4	+5V
8	Anode connection (-) of Turbo LED (with 18)
9	Reset switch (with 19)
10	Hard Disk LED input (with 20)
11	Power LED
12	N. C.
13	Ground
14	Keylock
15	Ground
18	Cathode connection (+) of Turbo LED (with 8)
19	Reset Switch (with 9)
20	Hard Disk LED input (with 10)

5.4 Speaker Connector: J6 (Pins 1-4)

Pins 1 – 4 of the 20-pin connector, J6, provide an interface to a speaker for audio tone generation. This connector provides four pins but only two pins are used. A speaker with 8-ohm or higher impedance is recommended.

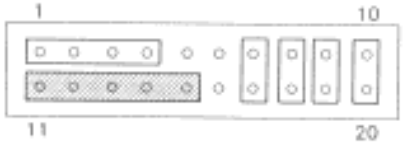
J6 orientation



J6 Pin #	Function
1	Speaker Out
2	N. C.
3	Ground
4	+5 Volts

Note: Orientation is not required when connecting a speaker to pins 1 – 4 of J6.
Note… What do they mean by this??? I would think the positive (+) of the speaker goes to pin 1, and the negative (-) of the speaker would be ground pin 3.

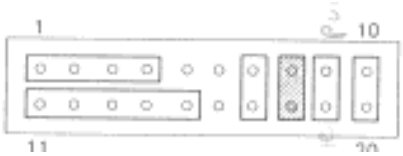
5.5 Power LED and Keylock Connector: J6 (Pins 11-15)



J6 Pin #	Function
11	Power LED
12	N. C.
13	Ground
14	Keylock
15	Ground

Pins 11-15 of the 20-pin connector J6 allow the user to connect the power LED and keylock switch of the system's front panel. The power LED indicates the *ON/OFF* status of the system. The keylock switch, when *CLOSED*, will disable the keyboard function.

5.6 Turbo LED connector: J6 (Pins 8 & 18)

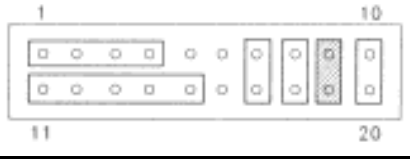


J6 Pin #	Function
8	Anode (-)
18	Cathode (+)

Pins 8 & 18 of the 20-pin connector J6 provide the user with an interface for connecting a turbo LED indicator in the system's front panel.

This LED, when on, indicates the Turbo (full) speed mode of the PCI54PV system.

5.7 Reset Switch connector: J6(pins 9 & 19)

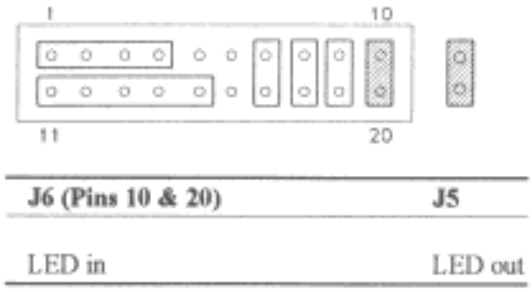


Pins 9 & 19 of the 20-pin connector, J6, provide an interface for a reset switch. The reset switch allows the user to reset the system without turning the power switch off and on.

To reset the PCI54PV based system, short pins 9 & 19 of J6 by pressing the reset switch of the system chassis.

Note: Orientation is not required when connecting a reset switch across pins 9 and 19 of J6.
Note: This should be obvious, but you want a push button switch and not a toggle switch. Also, you would want a push button, normally open switch. This type switch will short when pressed, and be open when not pressed.

5.8 Hard disk Access LED Connector: J6 (Pins 10 & 20), J5



These connectors allow the user to connect the hard disk access LED on the system's front panel. The LED will be on whenever the system is accessing the hard drive.

Connect the 2-pin connector from the system chassis to pins 10 & 20 of J6. Also, make a connection from J5 to the hard disk controller's LED interface.

Note: You may also connect the HDD LED on the system's front panel directly to the hard disk controller's LED interface without using these connectors.
Note: To me this diagram above looks backwards. I would think the connection from the hard disk controller would be labeled LED in due to it is getting a signal from something, hence heading in. I supposed they labeled it to match what it might say on the hard disk controller, which would say LED or LED out.

5.9 Installing a P54C/CT Processor

Skip this section of there is a P54C/CT processor already installed in U54 of the PCI54PV.

The PCI54PV is designed to accommodate a 75MHz, 90MHz or 100MHz P54C/CT processor. The P54C/CT processor, once installed, will be driven by an oscillator installed in OSC2 by a 3:2 (or 1.5x) frequency ratio. *Therefore, for a 75MHz P54C/CT processor, a 50MHz oscillator must be installed in OSC2. For a 90MHz P54C/CT processor, a 60MHz oscillator must be installed in OSC2. For a 100MHz P54C/CT processor, a 66 MHz oscillator must be installed.*

Note: *On my board I have found JP9 can set the CPU speed jumper. Since the board is fixed for a 3:2 (or 1.5x) ratio, the only way to installed different processors is change the bus speed. Note there are values that can be set but would be of little value other than testing.*

*The bus speeds marked with a * are the design speeds of the board, P75, P90 and P100. About the only thing you can overclock to is P120, but with an 80MHz bus, things may or may not work properly all the time. Remember that PCI and ISA peripherals and memory built when this board was aren't designed to run that high although some may without a problem.*

You can bump your P90 up to P100 without a problem. I did it for 2 years.

CPU Speed Jumper: JP9

JP9	Pentium chip speed	Bus speed
000	33 MHz	22 MHz
001	40 MHz	26 MHz
010	90 MHz	*60 MHz
011	60 MHz	40 MHz
100	75 MHz	*50 MHz
101	100 MHz	*66 MHz
110	120 MHz	80 MHz
111	50 MHz	33 MHz

There are three jumpers associated with JP9. The zero (0) above indicates open or off. The one (1) above indicates shorted or on.

This is a socket 5 motherboard with zero insertion force. Open the lever, and gently set the CPU in the socket taking care not to bend the pins. There is a diagonal set of pins holes (looks like a corner of the square is cut off) which will line up with the corresponding pins on the CPU chip. This is how you know which way to orient the chip. Also, if your chip doesn't have one attached, remember to use a heat sink or heat sink and fan. Attach the heat sink with thermal grease to increase the heat conductivity from the chip to the heat sink above.

Caution: The P54C/CT is specified to operate at a specified range of temperatures. Refer to the P54C/CT data book or consult the board manufacturer for details on the thermal specifications of the P54C/CT processor.
Note: The older Pentium chips were designed for an outer case temperature of 70°C. Info on how to measure this at the time of this writing could be found in the document:

http://developer.intel.com/design/intarch/manuals/241428.htm

5.10 Battery Selection: JP1

JP1: Battery Selection

: Clear CMOS RAM

: Use an external battery connected to J2

: Select on Board battery

5.11 LDEV# Sample Selection: JP4


SHORT: END OF SECOND T2


OPEN: END OF FIRST T2